Microscale thermoelectric devices for energy harvesting and thermal management

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Abstract

Superlattice material technologies in the Bi_2Te_3-material system can potentially enable efficient micro-scale thermoelectric devices for energy harvesting and active site-specific thermal management from ~200K to ~400K. The state-of-the-art in these thin film materials and the state of transition of these materials into device prototypes are presented. In the energy harvesting area, early results portend well for powering sensors and bio-implants, harnessing naturally occurring temperature gradients. Cooling of hot-spots (with flux levels > 1000 W/cm^2) in high power electronics appears feasible along with all solid-state micro-cooling down to 207K.

Keywords: Thermoelectrics, thin-film superlattices, energy harvesting, active thermal management, bio-thermal batteries

1 - INTRODUCTION

The US Department of Defense has been supporting the resurgence of the once-sleepy field of Thermoelectrics during the past decade, since the first set of ideas using nanoscale materials [1] were proposed at the National Thermogenic Workshop in 1992. In particular, the Office of Naval Research, the Defense Advanced Research Projects Agency and the Army Research Office have helped make impressive strides in the materials figure-of-merit, denoted as ZT, using nano-scale material concepts. Higher ZT of the thermoelectric materials can directly lead to improved efficiencies for both solid-state refrigeration and thermal-to-electric power conversion devices. There have been several reports [2, 3, 4] of enhanced ZT at various temperature regimes using superlattices, quantum-dots, and nano-crystalline inclusions, respectively. In combination with semiconductor technology tools for device fabrication, these materials offer unprecedented advantages such as high cooling power density and high-speed cooling/heating in thermal management and high specific power in direct thermal-to-electric power conversion systems. The improvements achieved with these nano-scale thermoelectric materials and their devices are timely for meeting many emerging needs in DoD systems as well as in commercial electronic and optoelectronic systems, in the areas of microscale thermoelectric devices for energy harvesting and active thermal management.

2 - NANO APPROACH TO ENHANCING ZT

Nanoscale thermoelectric materials, using phonon-blocking / electron-transmitting superlattices in thin-film form [2], using quantum-dot superlattices in thick-film form [3] and using nanoscale inclusions in bulk material form [4], increasingly appear to be the route to achieving enhanced ZT in thermoelectric materials. Superlattices in various material systems, using the concept of phonon-blocking/electron transmission [5] are being developed for various temperature regimes to enable thermal management or power harvesting at those respective temperatures. Bi_2Te_3-based superlattices [2] are useful below 175°C while PbTe-QD superlattices [3] PbTe/PbTeSe superlattices [6] are useful between 175 to ~300°C range, while Si/Ge superlattices [7] and ErAs:InGaAs/InGaAlAs quantum-dot superlattices [8], are likely to offer enhanced ZT, compared to bulk materials, in the 300 to 500°C range.

The engineering of thin-film thermoelectric superlattices and quantum-dot superlattices into useful devices can be implemented easily if the electric transport occurs across the superlattice interfaces, i.e. along the thickness of the film. This way, planar semiconductor device technology using standard microelectronic tools can be used. In the following sections, we specifically discuss the superlattice thermoelectric technologies in the Bi_2Te_3-material system. We discuss the state-of-the-art in these materials and highlight the state of transition of these materials into device prototypes for both microscale energy harvesting and high heat-flux active thermal management.

3 - BI_2TE_3-BASED SUPERLATTICE MATERIALS AND DEVICE TECHNOLOGY

The nanoscale superlattices (Fig. 1) are grown by metallorganic chemical vapor deposition (MOCVD). In-situ ellipsometry has been used to gain further control over nanometer-scale control of deposition. The MOCVD process

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can be scaled to multi-wafer growth and for large-area growth, similar to that for III-V semiconductor space photovoltaics - for enabling low-cost, volume production of modules. The fabrication of thin-film modules employ standard semiconductor device manufacturing tools such as photolithography, electroplating, wafer dicing and pick-and-place tools. This allows scalability of the module fabrication, from simple modules that can pump a few Watts of heat to multi-connected module-array that can pump tens of Watts.

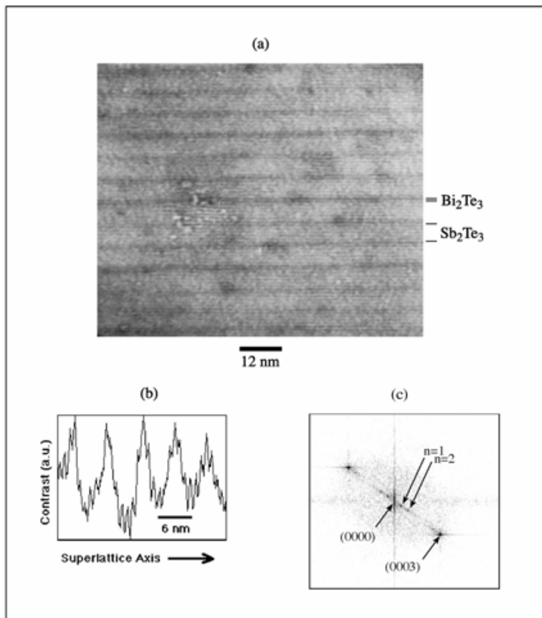

Figure 1: a) TEM image of a $10ÅBi_2Te_3/50ÅSb_2Te_3$ superlattice grown by MOCVD; b) image contrast oscillations at 1 nm scale and c) Fourier transform of the image showing superlattice electron diffraction spots.

4 - ENERGY HARVESTING

Thermoelectric power generator offers a unique and attractive alternative to conventional battery due to its waste heat energy harvesting capabilities. It is especially suited for many low power and portable applications such as supporting remote sensors and wireless devices. Thermoelectric generator's output voltage is direct proportional to temperature difference between its two junctions. In many cases, the obtainable temperature difference is less than 10K and the output voltage of a thermoelectric generator is usually a small fraction of a volt but at large current. Owing to many practical applications requiring higher voltage, a DC-DC step up converter may be required. Our results indicate that low-temperature energy harvesting can be simplified.

4.1 - Typical power requirements for sensors and bio-implants

All implantable medical devices (IMDs), including pacemakers, defibrillators, drug infusion pumps, and neurostimulators require electrical power. Non-rechargeable batteries are used as the source of power in most (IMDs). One limitation of IMDs is the longevity of the battery source. When the battery is unable to provide adequate power to the IMD, the IMD must be explanted and either the battery or the IMD replaced. The lifetime of the battery depends on the power requirements of the IMD and the amount of power stored in the battery. Implantable neurostimulators and pumps consume power at a higher rate than pacemakers. Consequently, the lifetime of neurostimulators is much less than that of implantable pacemakers. Temperature differences which exist either between the inner surface of the skin and the core body temperature or within the implantable device (see figure 2) could be used to produce electrical power, store energy as well and hence increase the battery life.

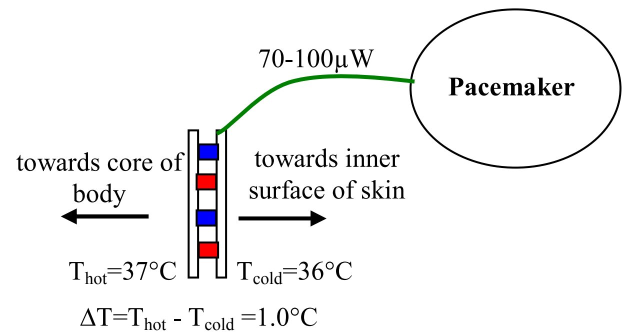

Figure 2: Schematic of a TE device taking advantage of a ΔT across the device to supply power to the pacemaker

4.2 - Energy Harvesting using temperature gradients from 2K to 200K

Shown in Figure 3 is an example of a 4x4 array of p-n couples using the thin-film superlattice materials. This array is about 2.5 mm x 2.5 mm x 0.3 mm. These modules have produced over 1 Watt of electric power, when an external ΔT of about 200K is applied across the two ends of the 0.3 mm thick module. This implies an areal power density of 16 W/cm^2; a volumetric power density of over 50 W/cm^3; a specific power of almost 100 W/gm.

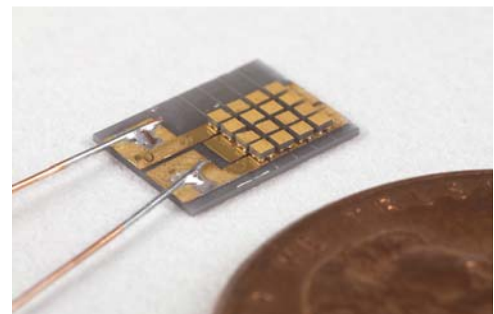

Figure 3 – A 4x4 module array made using 16 p-n couples made using the superlattice thin-film materials; the module is approximately 2.5 mm x 2.5 mm x 0.3 mm in dimensions.

Larger arrays of mini-modules, like the 4x4 array shown in Fig. 3, can be stringed together – with the couples being electrically in series and thermally in parallel – to produce

larger power levels. Shown in Table 1 is data from a 2.0 cm x 2.3 cm x 0.3 mm multi-module array (MMA) for a range of hot-side and cold-side temperatures. We note that the MMA produces as much as 1.25 Volts and a power of 31 mW, with a temperature differential of only 5K. The power harvesting load lines obtained from these MMAs, for temperature differentials <10K, are shown in Figure 4. Note that for small ΔT of 5K, we can generate over 31 mWatt at an open-circuit voltage of 1.25V; these are useable for a variety of sensors and wireless electronic devices.

Thot (°C)	Tcold (°C)	ΔT(C)	Power (W)	Voc(Volt)	Isc(A)	Pd (W/cm^2)
25.54	23.52	2.02	0.005	0.52	0.038	0.0
29.26	24.26	5	0.031	1.247	0.098	0.0
33.46	24.48	8.98	0.107	2.33	0.184	0.0
44.55	24.94	19.61	0.531	5.253	0.404	0.1
79.04	31.33	47.71	2.48	11.251	0.88	0.5
98.76	36.98	61.78	4.63	14.71	1.26	1.0
110.86	44.42	66.44	6.6	15.85	1.665	1.4
128.16	48.67	79.49	10.68	19.96	2.14	2.3
156.92	56.71	100.21	14.6	22.38	2.61	3.2

Table 1 Power generation characteristics of a 512-couple multi-module-array, packed in a 2.0 cm x 2.3 cm area, and with a height of ~0.3 mm, for various hot-side and cold-side temperatures. Note that the cold-side temperature is allowed to drift up, as more heat flows through the thin-film thermoelectric module, to enable easier rejection to an eventual heat-sink.

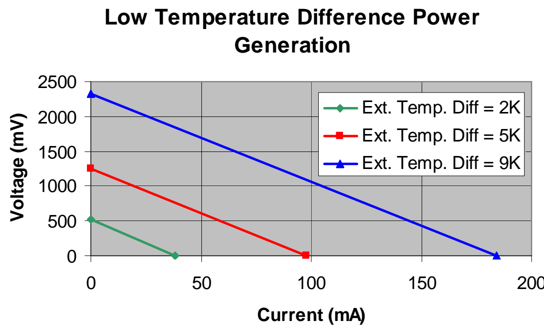

Figure 4 – Power generation characteristics of a 512-couple module, occupying a foot-print of 2.0 cm x 2.3 cm and ~0.3 mm height, for <10K; such power levels in the range of 5 mW to 100mW are useful for a variety of sensors and actuators.

5 - HIGH HEAT FLUX ELECTRONICS THERMAL MANAGEMENT

High performance, typically multi-GHz microprocessor chips from most manufacturers, face significant thermal management problems [9, 10], referred as hot-spots. For example, active chip portions such as the clock buffer unit and load storage unit [10] can have much higher power densities than the rest of the chip. These units, ranging in dimensions from tens of microns to a mm on a side, compared to the overall chip size of 1.5 cm on a side, can have hot-spots of about 5 to 10°C hotter than the rest of the chip. These hot-spots determine the ultimate performance as well as reliability of the entire chip. As the chip makers move to the 65 nm node and below, with multiple cores, the chips are facing issues with more hot-spots, which have to be managed for both reliability and performance [9]. While spray cooling and jet impingement techniques have been the mainstay for the thermal management of high-performance chips for the military electronics, such solutions are not commercially adoptable, and are likely to be inadequate for advanced mobile electronics.

Several advanced passive thermal management solutions based on fluid flow through micro-channels and magneto-hydro-dynamic pumping of heat-transfer liquids have been developed. These have generally relied on Si-micromachining techniques; but they are expected to be inadequate for the long haul to meet more demanding requirements in the future. These requirements include higher-density heat fluxes at the hot-sot, multiple hot-spots, cooling-on-demand, ultra-low-profile solutions, and overall system efficiency. In fact, some of the advanced passive thermal management solutions being developed at a macroscopic level along with advances in thermal interface materials being developed by various electronics component manufacturers would complement the advanced active thermoelectric cooling technologies. Figure 5 reproduces the summary analysis [9] of various cooling techniques to manage these hot-spots. This clearly shows that, both based on volume constraint and cooling capability offered, micro-scale embedded e-TECs [11, 12] can offer one of the best solutions. Hot-spot cooling (by >5°C) at a flux level of >1000 W/cm^2 has been achieved [11]. Further, the 90% rise time associated with hot-spot creation in high-performance chips can be in the range of tens of milliseconds to a couple of hundreds of milliseconds, with smaller and asymmetrical circuit units tending to becoming hot-spots sooner [10]. Under these conditions, the high-speed cooling capability of thin-film thermoelectric devices [2] will likely be unparalleled.

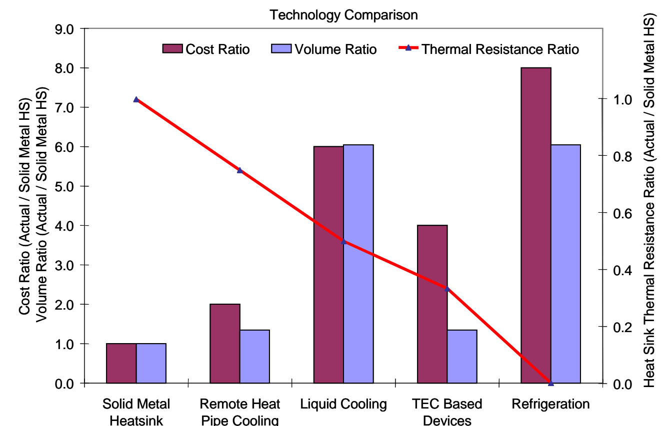

Figure 5 – Cooling characteristics of various potential solutions to manage hot-spots in microprocessors [from Ref. 9].

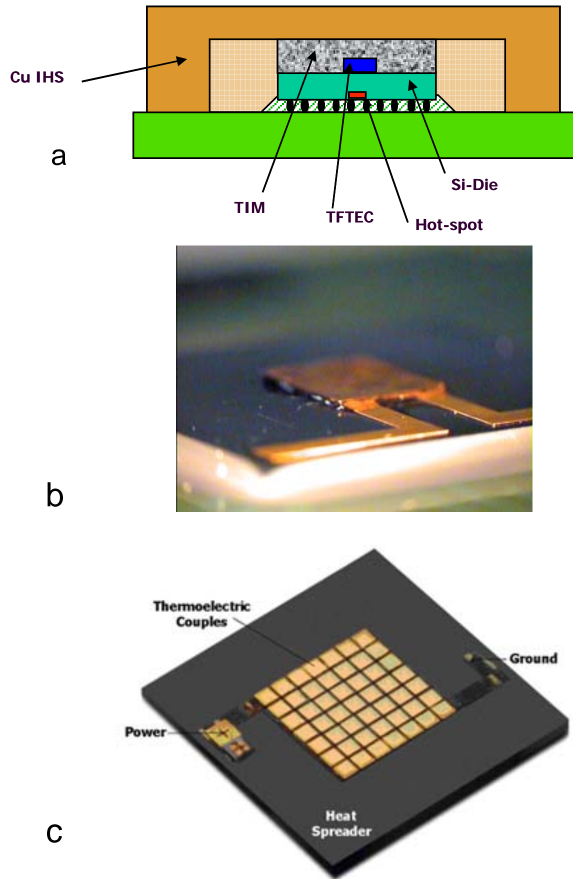

Figure 6 – a) Schematic arrangement of a thin-film cooler on the backside of a chip and fitting within a conventional electronic package; b) a 10 Watt cooler, with total height of only 100 microns, mounted on the backside of a Si wafer; the 2.5 mm x 2.5 mm cooling module is directly below a hot-spot on the front side of the active Si wafer [11]; c) a 3 mm x 3 mm x 0.1 mm cooler fabricated on an integrated heat-spreader typically used for a high-performance chip [12].

Beyond electronics, thermal management of optoelectronic packages for both long-haul and short-haul fiber-optic communication lasers as well as for integrating lasers within high-density electronic systems requires extremely small foot-print thermoelectric coolers. In addition to high coefficient of performance (COP) at fairly large temperature differentials, these coolers need to pump large heat-flux levels in excess of 100 W/cm^2 at the module level. Our smallest module physical dimensions were 1mm (L) x 1mm (W) x 0.5mm (H), capable of pumping well over 2 Watts. In slightly larger, 2.5 mm x 2.5 mm x 1mm size modules, heat pumping capacities of up to 10 Watts have been measured, translating to a cooling power density of 160 W/cm^2 at the module-level. The potential applications for such modules are in laser diode cooling in various small packages such as in TO cans and in some highly-integrated optoelectronic packages.

6 - MICRO-CRYOGENIC THERMAL MANAGEMENT

The electronics industry also could benefit from solid-state cryogenic cooling that can cool targets down below 200K. Current bulk thermoelectric devices are limited to a cold-side temperature of about 170K, are capable of only small heat fluxes and can have profile thickness in the range of several centimeters. Significant progress has been made in overcoming electrical and thermal parasitics, that are unique to thin-film thermoelectric devices, to achieve ΔT_{max} of 55K (T_{cold} ~240K) in single-stage devices [13]. We have also measured a ΔT_{max} of 90K (T_{cold} ~207K) in low-profile (<2 mm thick), three-stage thin-film thermoelectric devices. The area of micro-cooling can be localized to ~500 µm x 500 µm or smaller. These developments in combination with MEMS concepts can be useful for cooling low noise amplifiers, infrared focal-plane arrays, quantum cascade lasers, etc.

ACKNOWLEDGMENTS

This work was supported by the DARPA/Defense Science Office through the US Office of Naval Research (2003-Current) and the US Army Research Office (2000-2003). The authors acknowledge the support of Nextreme Thermal Solutions for the fabrication of the thin-film modules and Fig. 6c. Dr. Mahajan of Intel Corporation is thanked for providing data of Fig. 5.

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