Hybrid Thermoelectric Conversion for Enhanced Efficiency in Mobile Computing Platforms

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Abstract

Hybrid Thermoelectric Conversion (HTC) has been deployed as the means to improve the efficiency of high performance mobile computing systems. HTC utilizes the thermal margin in the cooling solution, when the electronic component is not fully active, to integrate a Thermoelectric (TE) module into the heat dissipation path for energy scavenging. When the component is driven to its junction temperature limit through a heavy workload, the same TE module is switched to refrigeration mode to provide additional cooling headroom for improved performance. A set of semi-realistic system usage assumptions and parameters have been utilized for the evaluation of HTC in system environments. Results from finite element analysis (FEA) simulation of the topology, and full TE characterization are shared. Common TE models are then used to build an iterative system solver to estimate up to 10% system efficiency benefit from HTC integration.

Keywords: Efficient computing, Hybrid thermoelectric conversion, Sustainable thermal management

1 - INTRODUCTION

The performance of mobile computing platforms is limited by the maximum system power they are allowed to dissipate without exceeding outer skin and device junction temperature requirements [1, 2]. Average power consumption is also paramount due to its impact on battery life. Much work has been done to address system power and efficiency [3, 4]. However, application of energy scavenging and conversion methods has been limited. One such source is heat energy generated by device switching in system components.

Usage of Thermoelectric (TE) modules for electric generation has various problems. First, traditional TE materials have low energy conversion efficiency. Second, thermal resistance of the heat dissipation paths increases once the TE module is inserted for energy scavenging. The shunt path approach developed in [5] reduced this impact, but the cooling capacity was still penalized by 10-15 W. A constant heat source was used to demonstrate the potential for powering up a custom (low-power) cooling fan in the vicinity of the microprocessor, but additional problems were identified with this closed-loop configuration due to dynamic behavior of a real microprocessor, and required start-up power for the fan.

In this work, TE conversion techniques have been applied with a hybridized approach. The opportunity of having better microprocessor and chipset cooling solutions in the platform than needed by most workloads is converted to battery life benefit through integrated TEs. The scavenged energy is stored to the battery when charging, and is used to supplement external supply when not charging. The utility of thermoelectric modules on microprocessors as both generators and refrigerators has been analyzed. The configuration is particularly suitable to high performance notebook systems that need to satisfy the dichotomy of a battery and a performance mode. Hybrid Thermoelectric Conversion (HTC) system is a scavenger when performance is not needed, and turns into a performance booster when thermally limited applications are being executed.

Insight into main modes of usage is crucial to designing an effective system solution. Semi-realistic usage assumptions are therefore discussed in the next section for the purposes of notebook thermal management and battery life evaluation. Integration of HTC to notebook systems is presented in Section 3. Expected system benefits and impacts are quantified in Section 4 using real thermoelectric module characterization data. Conclusions and future work are summarized in the final section.

2 - HIGH PERFORMANCE MOBILE COMPUTING

Two fundamentally different modes drive the assumptions behind mobile computer design today. First is the average power used to calculate battery life. Second is the thermal design power for evaluating the cooling solution.

2.1 - Average Power for Battery Life

Average power distribution in portable computing platforms is dominated by the LCD display as shown in Fig. 1, and not by the CPU, due to built-in advanced power management features. Total average power with standard battery life benchmark [6] in such a system is 11-12 W [2].

2.2 - Thermal Design Power (TDP) for Cooling

The cooling solution accounts for a worst case realistic activity across the platform, which results in scenario

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depicted in Fig. 2. Total Thermal Design Power (TDP) for a typical system is around 50 W. The difference between the user ambient and the junction temperature of the CPU has to remain ~65 °C [2]. As shown in the figure, CPU is overwhelmingly dominant in driving the worst case power.
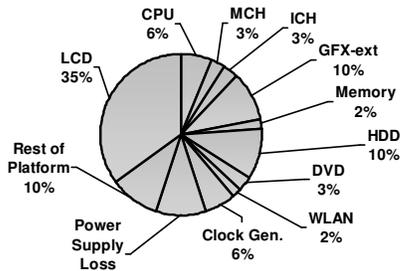
Figure 1 – Mobile platform average power distribution [2]
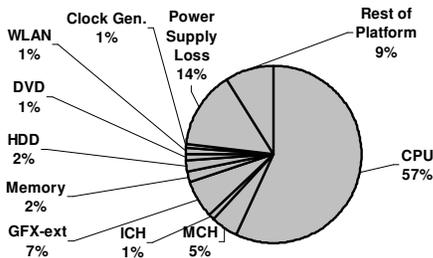
Figure 2 – Mobile platform Thermal Design Power [2]

2.3 - Semi-Realistic Usage Model

There is a range of other scenarios executed on a system at a given time, most of which dissipate power levels between those in Fig. 1 and Fig. 2. It is hard to analyze each case. Instead, a semi-realistic workload has been designed around the power numbers from [2] for the purposes of TE integration around two higher power (and higher power density) components: CPU and Integrated GMCH (Graphics with Memory Controller Hub) chipset. Figure 3 shows this workload. There are 4 activity scenarios of interest.
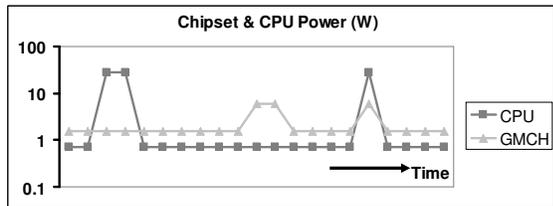
Figure 3 – Workload model with 4 distinct scenarios

3 - HYBRID THERMOELECTRIC CONVERSION

It follows from previous work [5] that TE generation used for maximum energy scavenging will result in performance degradation. Therefore, HTC architecture targets a particular notebook usage where both performance and battery life are

important. HTC boosts performance during peaks in Fig. 3 through refrigeration, and otherwise scavenges energy.

3.1 - System Topology

Since CPU TDP dominates the platform cooling budget (Fig. 2), hybrid operation mode is only supported on the CPU in this work as shown in Fig. 4. The TE module attached to the chipset (denoted as CS in the figure), only operates in generation mode. The nomenclature in Fig. 4 mostly follows conventional: Q represents heat load (W), Tj device junction temperature (°C), Th and Tc temperature (°C) at the hot and cold side of the TE module respectively, Ta ambient temperature (°C), RL resistive load model, Ψ thermal resistance (°C/W), PL delivered or generated power (W) to and from the TE module for refrigeration or generation mode of operation respectively. Tc_cpu temperature point can exceed Th_cpu temperature when the TE module is being used as a refrigerator. The existence of shunt heat path is very critical, as demonstrated in [7], to achieve reasonable heat loads without exceeding device Tj limits. This can be attained by integrating a TE module into the heat pipe in a way not to overlap the full component as shown in Fig. 5 (top).

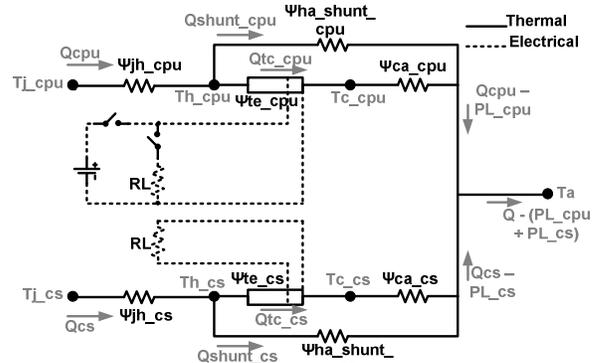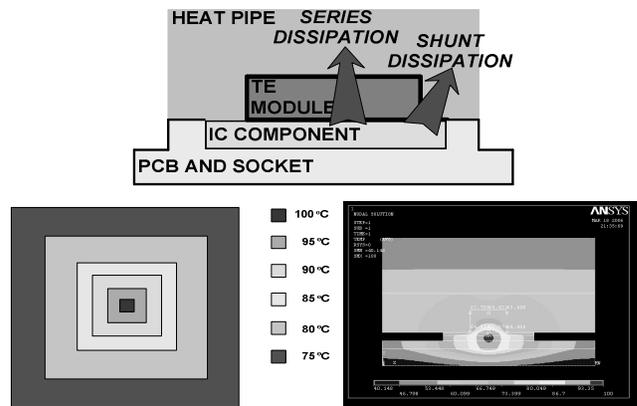**Figure 4 – HTC thermal and electrical network topology**

Figure 5 – Heat pipe with an integrated TE module (top) simulated using Finite Element Analysis (FEA) model of a non-uniform heat source (bottom left) to estimate series to shunt heat dissipation ratios from flux (bottom right)

3.2 - System Parameters and Models

All CPU related platform specifications extracted from the literature [2, 8] are summarized in Table 1. Some of the specifications, such as the thicknesses of the PCB are estimated based on the total platform size. The absolute parameter values will vary, but sensitivities are more important to understand for this study.

A thermal model has been used to estimate shunt thermal resistance under realistic non-uniform load conditions [9, 10] by integrating the TE into the heat pipe as in Fig. 5. An effective shunt thermal resistance value of 2-3 times that of the Ψca is attained on the shunt path, depending on TE thermal resistance. A reasonable average temperature drop is obtained across the TE module for electric generation (Eq. 1):

$$\Psi ha\_chunt\_cpu \sim 2 \text{ to } 3 \text{ x } \Psi ca\_cpu \qquad (1)$$

Table 1 – System specifications

Parameter	Estimate
Platform Size (inch)	10 x 12 x 1
CPU Package Size (mm)	35 x 35 x 1.5
CPU Die Size (mm)	15 x 15 x 1
PCB thickness (mm)	3
Metal plate thickness (mm)	7
Platform TDP Power (W)	50
CPU TDP Power (W)	28.5 (50W * 57%)
Maximum Tskin (°C)	50
Ta (°C)	35
Maximum CPU Tj (°C)	100
CPU TDP Ψja (°C/W)	2.28 (0.9 Ψjh + 1.38 Ψca)

The parameter estimates have been utilized next to evaluate the HTC system using the TE shunt path model developed in [7], and TE refrigeration models described in [11, 12]. The details of these models will not be reiterated in this text.

4 - HTC SYSTEM EVALUATION

### 4.1 - Thermoelectric Micro-Module Characterization

An off-the-shelf micro-module [13] of relevant dimensions for the desired application has been characterized in order to evaluate hybrid operation capabilities, and extract important TE parameters for system evaluation. The setup, depicted in Fig. 6, is similar to one described in [14] with OFHC copper replaced by aluminum blocks, cold plate by a cooling fan (top), and the heater by a hot plate (bottom).

TE module resistance, maximum theoretical power output, and seebeck coefficient have been measured using the techniques described in [15] and [16], for a range of ΔTs across the module. Higher ΔT corresponds to higher average TE temperature in the experiments. The dependence of the parameters to ΔT, shown in Fig. 7, is in line with the

expectations. Otherwise, the off-the-shelf component has a relatively poor Seebeck coefficient, and hence low efficiency compared to other modules noted in the literature.
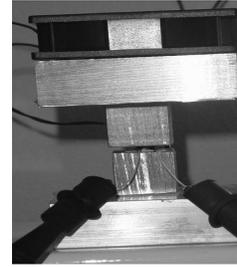
Figure 6 – TE micro-module characterization setup
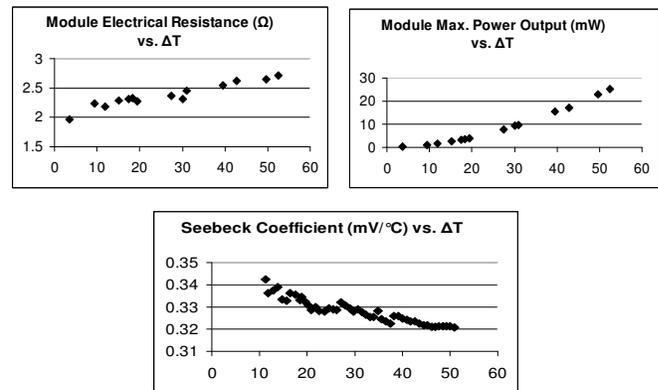
Figure 7 – Characterized electrical resistance, maximum power output (top) and seebeck coefficient (bottom) against forced ΔT across the TE module
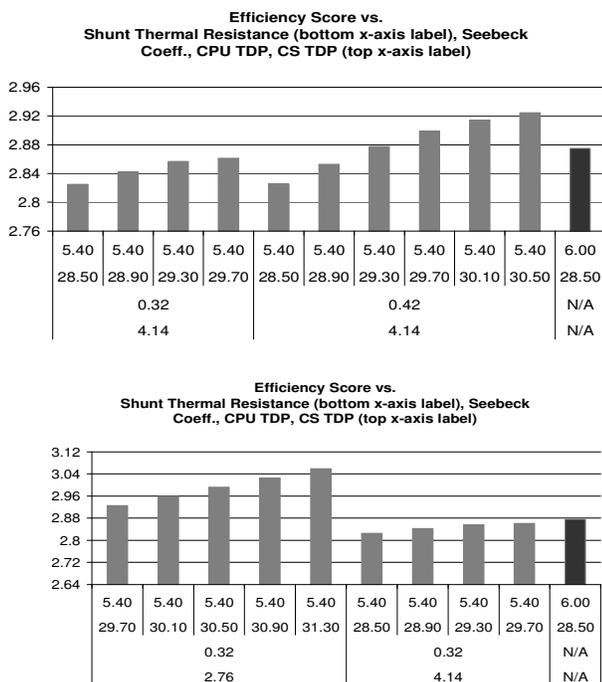
4.2 - Simple Efficiency Metric

Maximum dynamic power consumption in IC components is linearly related to clock frequency of the chip through $C.V^2.f$ formula [17] where C is the effective switching die capacitance, V is the supply voltage, and f is the frequency. Adding to that the size constrained mobile platform chassis, thermal design power (TDP) budget of a given component is highly correlated to the maximum performance it can achieve without violating its junction temperature specification. A simple performance/watt platform efficiency metric can therefore be devised by taking the ratio of maximum achievable TDP of the performance-critical components like CPU and Chipset to total platform average power calculated with the usage model from Fig. 3 (Eq 2.)

$$\text{Efficiency} = \Sigma \text{ Max Device TDP / Platform Avg. Power} \qquad (2)$$

4.3 - Notebook System Evaluation with HTC

The notebook has been simulated for HTC configuration with the help of a custom-built iterative solver. Figure 8 (top) depicts the variation of the efficiency score across two different values of the seebeck coefficient, a fixed minimum shunt thermal resistance that is 3x the case-to-ambient

thermal resistance, and various CPU and Chipset TDP values. The dark entry on the rightmost side is the baseline with no TE integration. The particular TE module characterized in the previous sections (0.32 mV/°C seebeck coeff.) can barely achieve the baseline efficiency score. Even though the maximum of 31.3 W CPU TDP should result in a significant performance improvement over baseline, its advantage is being offset by the platform average power impact of the refrigerator during peak activities. An incremental improvement of using a material with slightly higher seebeck coefficient (e.g. 0.42 mV/°C) results in better efficiency than the baseline. Figure 8 (bottom) also demonstrates a system with a lower shunt thermal resistance that is 2x the case-to-ambient. In this case, all efficiency scores simulated at the high end of the CPU TDP range exceed the baseline.

Efficiency Score vs.
Shunt Thermal Resistance (bottom x-axis label), Seebeck
Coeff., CPU TDP, CS TDP (top x-axis label)

Efficiency Score vs.
Shunt Thermal Resistance (bottom x-axis label), Seebeck
Coeff., CPU TDP, CS TDP (top x-axis label)

Figure 8 – HTC Efficiency improvements over baseline portable system

5 - CONCLUSIONS AND FUTURE WORK

HTC architecture has been presented for efficiency optimizations in high performance mobile computing. Semi-realistic usage assumptions and real notebook parameters have been employed for analysis. The integration of a TE micro-module into the heat pipe has been simulated using a FEA solver to quantify a feasible shunt thermal path. Characterization of an off-the-shelf TE module has provided insights into real TE operation in both generation and refrigeration modes. Finally, a simple efficiency metric was devised and deployed in an iterative solver to prove the overall benefit of the HTC approach with semi-realistic usage. It is estimated based on the studies so far that up to 10% efficiency score improvement is feasible with quality off-the-shelf TE components and careful system design.

Additional TE components with better efficiency will be characterized in future work. The design of the power electronics interface between the HTC and the system DC bus will be completed. Finally a real notebook system will be enhanced with HTC for a concept system evaluation.

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