HIGH SURFACE AREA DENSITY
NANO THIN FILM SOLID OXIDE FUEL CELLS

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Abstract: This paper presents the design and fabrication of a silicon-based solid oxide fuel cell (SOFC) with high surface area density in a limited volume. The structure consists of a corrugated nano thin film electrolyte and a silicon supporting layer on a two-stage silicon wafer through hole to maximize the electrochemically active surface area within a given volume. The 3 um silicon supporting layer is done by boron-etch stop technique with diffusion doping. The fabrication of two-stage wafer through hole combines deep reactive ionic etching (DRIE) and KOH wet etching of silicon for a wafer through hole containing two difference sizes. By these design and fabrication methods, the absolute electrochemically active area can be as high as five times of that of the projected area.

Key Words: thin film solid oxide fuel cells, atomic layer deposition, two-stage wafer though hole, boron etch stop

1. INTRODUCTION

Solid oxide fuel cells (SOFCs) utilize a range of ceramic electrolyte materials, with yttria stabilized zirconia (YSZ) being the most common choice. Due to the low oxygen ionic conductivity of solid electrolyte, traditional SOFCs need to operate at relatively high temperature (800-1000 degree centigrade). This limits the application of SOFCs to large scale, stationary applications. Operating SOFCs at low temperature decreases the electrolyte ionic conductivity; and consequently the power density of fuels cell is sacrificed. One effective way to lower the operating temperature is by reducing the electrolyte thickness to decrease the Ohmic loss. This can be achieved by deposition of submicron thickness electrolyte with thin film deposition techniques, such as sputtering or atomic layer deposition (ALD). These thin film deposition techniques also facilitate employing MEMS processes to fabricate micro scale SOFC structures. Our group first demonstrated a silicon-based micro SOFC with free-standing nano thin film YSZ electrolyte. The thickness of the electrolyte is 50 to 150nm. From a single cell we have reported power densities as high as 400mW/cm^2 at 400 degrees centigrade [1-2]. Such a low temperature SOFC opens the opportunities for portable applications.

Although the power density reported in [1-2] from a single MEMS fuel cell at low temperatures is high, the absolute power output is too low for practical use (The absolute power reported is at tens of micro Watts scale). This is due to the low electrochemically active surface area density. To effectively increase the surface area density in a limited volume, a corrugated nano thin film YSZ membrane was fabricated by our laboratory. [3] The YSZ is deposited by atomic layer deposition (ALD) on a 4" silicon substrate pre-patterned with 10-40um deep circular trenches. The YSZ replicates the pre-patterned surface profile and forms a corrugated electrolyte membrane after removal of the silicon substrate. The deeper the trench is, the higher the resulting surface area density.

Based on the corrugated thin film SOFC developed in [3], two new fabrication methods are presently explored to reinforce the corrugated electrolyte membrane and to further increase the usable wafer surface area. One is based on a heavy boron-doped silicon supporting layer, and the other comprises a two-stage wafer through hole. These methods and detailed fabrication process are described in this report.

2. EXPERIMENTAL

2.1 Fabrication Methods

Heavily boron-doped silicon supporting layer When silicon is doped with boron concentrations higher than $10^{19}/cm^3$, the etching rate in KOH of silicon decreases significantly, therefore is a good candidate as an etch stop in KOH etching [4]. By utilizing this boron etch stop technique, a few micrometer thick of silicon can be left after KOH etching to act as a supporting layer for the free-standing corrugated YSZ membrane fabricated in [3]. This provides a mechanical reinforcement of the corrugated thin film YSZ membrane and allows deeper corrugation. The concept is illustrated in figure 2(a).

Two-stage wafer through hole The two-stage wafer though hole enables the fabrication of a through wafer hole comprising two different sizes. The purpose of this method is to increase the usable wafer surface area while keep the free-standing membrane small. In a through-wafer etching with KOH solution, the crystallinity of (100) silicon wafer inevitably limits the opening on the top surface. The two-stage wafer through hole etching process combines a DRIE etching and a KOH etching. The anisotropic DRIE etching first etches through halfway the wafer thickness before reaching the pattern on the other side. The wafer through whole is then completed by KOH etching of (100) surfaces. The enhancement in surface area of the two-stage wafer though hole method, relative to KOH etching, is illustrated in Figure 2(b). The deeper the DRIE etching, the smaller the spacing between stage-II windows and the large the usable surface area. The improvement in percentage of usable surface area is much more significant for smaller stage-II holes.

By the combination of the two strategies mentioned above, the ultimate structure of the high surface area density fuel cell is illustrated in figure 2(c).

2.2 Fabrication Processes

The complete fabrication process is shown in Figure 3. A four inch silicon wafer is used as the
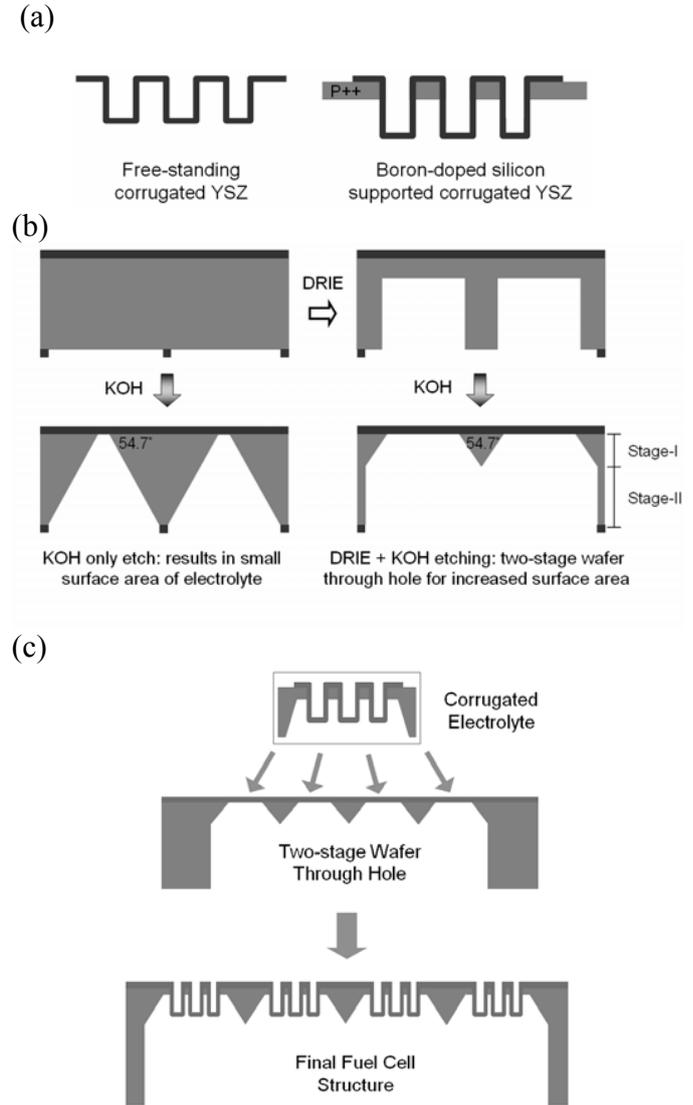

(a)

(b)

(c)

Fig. 2: Illustration of the two fabrication methods. (a) The addition of boron etch stop supporting layer helps to maintain the strength of the corrugated thin film and allows deeper thin film corrugation. (b) Comparison of usable surface area between etching by KOH only and by two-stage wafer though hole etching. (c) Final structure combining both fabrication methods

substrate for the SOFC structure. The wafer is p-type (100) double-side polished with 350-400μm in thickness. One surface is first doped with boron by diffusion doping at 1100 degree centigrade for 6 hours, with 1 um of silicon dioxide as doping mask. 1.6 um thick of photoresist (3612 positive resist from Shipley Co.) is then coated on the boron-doped side. Photolithography to make a

mask with circles arranged in close-packed layout to maximize the number of circles in the limited surface area. Circle sizes from 10 um to 65 um. The circles are etched with DRIE to make cup-shaped trenches. 100 nm of low stress silicon nitride is then deposited by low pressure chemical vapor deposition (LPCVD) on both sides of the wafer. The silicon nitride is then patterned with photolithography to form the stage-I window mask for KOH etching. The windows sizes are from 10mm to 60mm. A 7 um thick photoresist is coated on top of the silicon nitride stage-I mask and patterned with photolithography to make small window mask for DRIE. The edge of the outer most small windows have a 50~200um of distance to the silicon nitride mask edge. This is to prevent from a concaved shape of (111) surface after KOH etching. The wafer is etched with DRIE for 150 to 250 um in depth for the first step of wafer through hole. After removing the photoresist in piranha solution, the YSZ thin film electrolyte with thickness of 50-150nm is deposited on the cup-shaped trenches by ALD technique. The deposited YSZ replicates the pre-patterned surface contour of the circular trenches. To complete the two-stage wafer-through hole, the opened Si windows were etched in 10% KOH solution at 60°C. The etching will stop at the nitride layer and slow down at the heavily boron-doped silicon layer. The silicon nitride layer adhering to the electrolyte is then removed by SF$_6$ plasma etching. The active surface areas for electrochemical reaction are the YSZ cups bottom and partial cup side wall. Finally, porous platinum electrode/catalyst films (cathode and anode) were deposited on both sides of YSZ with DC magnetron sputtering.

3. RESULTS AND DISCUSSION

Figure 4 shows the images of the fabricated SOFC. In 4(a) a 4-inch silicon wafer with four SOFC chips are presented. Each chip contains four stage-I window, with eight stage-II window inside each of them. The sizes of the stage-II window fabricated are from 2mm by 2mm to 6mm by 6mm, where 3mm by 3mm size is shown here. Each stage-II window contains a sheer number of YSZ "cups," from several thousands to

Silicon dioxide
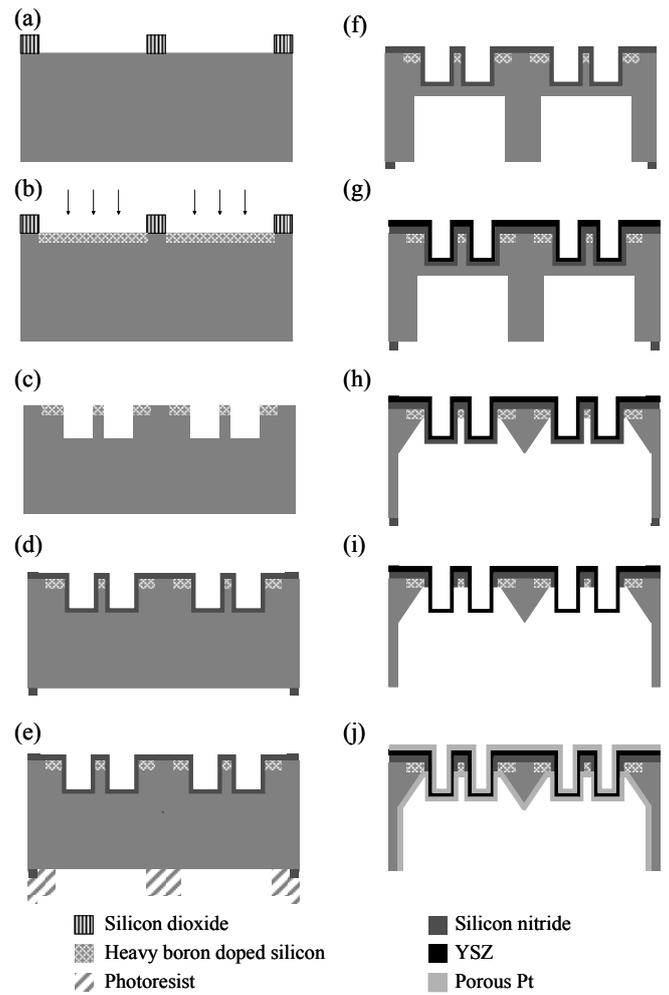Heavy boron doped silicon
Photoresist
Silicon nitride
YSZ
Porous Pt

Fig. 3: Schematic of fabrication process (a) Grow silicon dioxide mask for boron doping on P-type (100) silicon wafer. Wafer thickness is 350-400um (b) Diffusion doping of boron at 1100 degree C for 6 hours (b) Remove oxide mask and DRIE etching to pattern trenches on the doped surface. (d) Deposit silicon nitride on both side and pattern the nitride mask for large window. (e) Coat and pattern photoresist small window mask for DRIE etching. (f) DRIE etching the silicon substrate for 150-250um deep. Remove photoresist. (g) Deposit 50-150nm of YSZ on the boron-doped side with ALD. (h) KOH etching to open the large and small window. The etching will stop at the high concentration boron doping layer and silicon nitride. (i) Plasma etching to remove silicon nitride. The YSZ "cup" bottom and part of the cup sidewall is exposed as a free-standing thin film. (j) DC sputtering porous platinum as catalysts and electrodes.

several hundred thousands depending on the window size. The spacing between stage-II windows are from 200 to 410um, depending on the design and on the depth of etching in step (f) in figure 3. This spacing is larger than 550um if only KOH etching is used, so the reduction of the spacing is obvious and the increasing in usable wafer surface area is particularly significant for smaller sizes of windows. Figure 4(b) shows the cross-section view of the corrugated membrane supported by the boron-doped silicon layer. For the image shown here, the cup depth is 10um (maximum depth fabricated is 40um), and the supporting layer is about 3 um thick. The suspending porous-Pt/YSZ/porous-Pt membrane is 120nm/80nm/120nm, respectively.
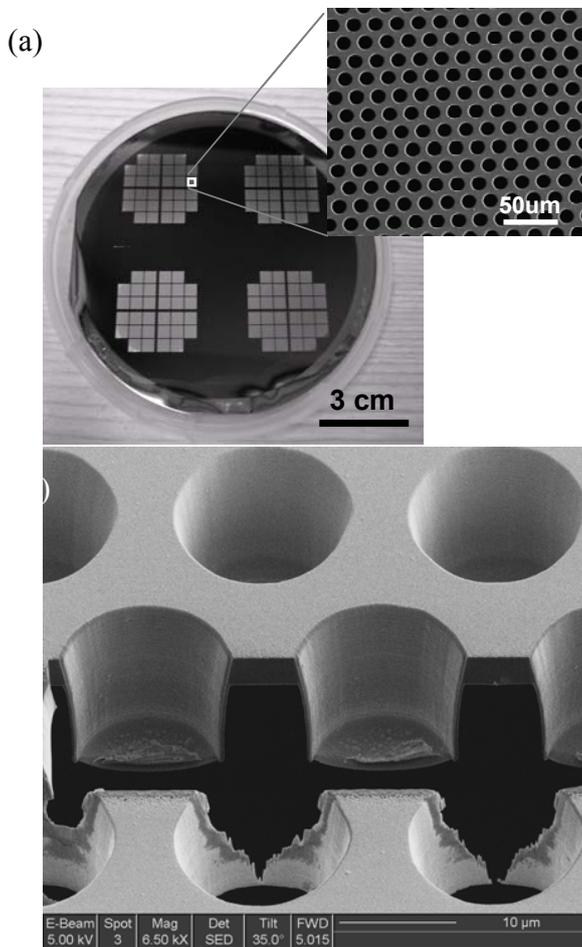

(a)

Fig. 4: (a) The fabricated SOFC on a four inch silicon wafer. Each window contains a sheer number of cups. (b) Thin film YSZ cups with silicon supporting layer. (Cup damage came from the ion-milling of focus ion beam to open the membrane.)

Comparing to the freestanding corrugated YSZ SOFCs without the silicon supporting layer, some electrochemically active area are covered by the silicon supporting layer in this SOFC and cause some area loss. However, with the aid of the silicon supporting layer, the cup can be made deeper to gain extra surface area while the strength of the membrane remains. Also, extra usable wafer surface area is gained from larger window sizes and smaller spacing between stage-II windows. These compensate the surface area loss from the silicon supporting layer. Overall the absolute surface area can be up to five times of the projected area from this design.

4. CONCLUSIONS

We have successfully fabricated nano thin film SOFCs by using MEMS fabrication methods, including boron-etch stop technique and two-stage wafer through hole. The boron-etch stop provides a stable support for the YSZ thin film electrolyte and allows 3mm by 3mm to 6mm by 3mm of free-standing membranes hanging over the through-wafer window. The two-stage wafer through hole technique reduces the spacing between etch window and increases the usable wafer surface area. Fuel cell performance of this MEMS SOFC will be characterized in the future. The present SOFC architecture may open new applications for SOFCs in transportation and portable microelectronic devices with sufficient absolute power output. .

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