

RING OSCILLATOR CONTROLLED ASYNCHRONOUS CHARGE-PUMP FOR LOW POWER RENEWABLE APPLICATIONS IN COMPUTING PLATFORMS

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Abstract: The success of integrated renewable energy sources in mobile computing systems highly depends on low cost, low area, and efficient power conversion schemes. Various boost implementations have thus been analyzed in this work for suitability to the application of energy scavenging from low power photovoltaic and thermoelectric sources. A new two stage charge pump topology and an asynchronous controller are proposed as a result. The implementation has been verified through simulations, and validated through sample proof of concept measurements. The data confirms the feasibility of implementing a compact LSI power electronics chip to extend battery life in mobile systems.

Key Words: asynchronous charge pump, ring oscillator control, renewables in mobile computing

1. INTRODUCTION

Environment friendly Energy Star computer initiative by EPA [1] is taking effect this year. The computing systems with Energy Star logo will consequently have a fixed maximum power consumption allowance, when idle. Adding to that the focus to extend the battery life in the mobile industry [2], advanced power management modes in computers are emphasized more than ever.

We took a new power management approach in previous work [3] by using photovoltaic (PV) and thermoelectric (TE) renewable sources to improve system efficiency. We shared an enhanced power architecture [4] to integrate renewable sources into the most sustainable mobile systems. We demonstrated power conversion based on conventional boost worked for sufficiently high operating voltages, but had very poor efficiency.

It was concluded during the early investigations that low cost, low area, and efficient boost converter design is the key to making the energy scavenging initiatives the next revolution in green computing technologies. However, there is little work in the DC-DC boost conversion when the power sources are in milliWatts (mW) range. The desirable properties of the controller and the resulting design choices are hence discussed next in this paper. Section 3 covers relevant boost performance metrics, and the resulting boost converter topology using these. A two stage charge pump topology with a simple asynchronous controller is thus developed. Section 4

contains simulation and prototype results summary. Finally, conclusions are in the last section.

2. CONTROLLER

2.1 Requirements

Renewable sources are intermittent, as demonstrated by the ranges provided in Table 1 [4]. Extraction of power from the TEs poses an additional challenge due to the low power levels. Hence, the remaining discussion will focus on boost implementation for the TE modules in the system. Three requirements have been identified for the design of the TE boost controller:

- i) The number of power consuming transistors should be minimized. The implementation should be simple to avoid diminishing returns.
- ii) A boost stage should turn on only if the corresponding control will consume less power than the power generated at the stage output.
- iii) The controller power dissipation should scale with TE power output in order to enable net positive energy scavenging under low power conditions. When the minimum power generation requirement from (ii) can no longer be met, the controller should turn off.

Design Range	I (mA)	V (V)	P (mW)
TE	0-50	0-0.5	0-25
PV	1-100	0.5-5	0.5-500

Table 1: Current, voltage, and power range for TE & PV sources in Thin & Light systems [4]

2.2 Design

A simple controller topology resulting from the above requirements is depicted in Fig. 1. Each boost stage has its own asynchronous controller unit with a minimum number of devices to satisfy requirement (i). An ON threshold is set through the resistor divider at the input of each comparator based on requirement (ii). Once the comparator trips, an asynchronous pulse generator is enabled. The operating frequency is lowest when the TE output voltage barely exceeds the ON threshold.

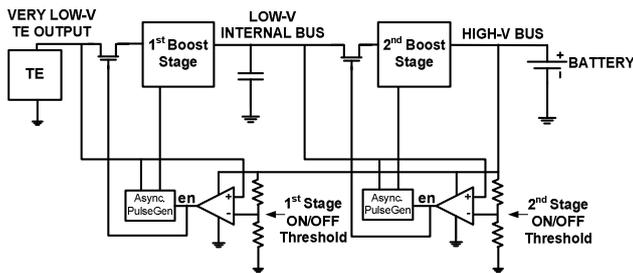


Fig. 1: An asynchronous converter topology

The voltage sensing asynchronous pulse generator is implemented through a simple CMOS ring oscillator with an enable input (see Fig. 2.) As the voltage (and power) available from the renewable source increases, CMOS gate delay decreases, and the ring oscillator operates at higher frequency with higher power dissipation. The controller dynamic power is linearly related to the frequency, and has second order dependence on voltage:

$$\text{Pulse Generator Dynamic Power} = C \cdot V^2 \cdot f \quad (1)$$

C in the equation stands for switching parasitic and load capacitance, V for voltage, and f for switching frequency. Hence, the controller dynamic power dissipation has a cubic dependence on TE power output, and meets requirement (iii). The circuit used for threshold generation is not powered by the renewable source. The associated power dissipation can be optimized since the bandwidth requirements are low. Alternatively the threshold circuit can be fully integrated by designing a minimum power detection capability into the pulse generator, for example using MOSFET ON threshold voltage (V_t) available from the device technology. A low V_t CMOS technology is required by the ring oscillator in order for the controller to turn on at low TE output levels. Al-

ternatively, body biasing techniques can be utilized to program V_t , which would in turn translate to a programmable ON threshold.

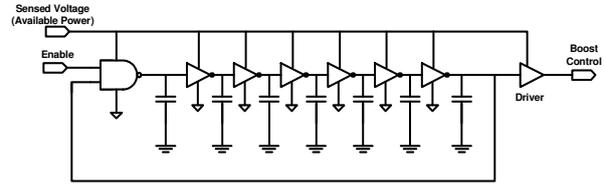


Fig. 2: Ring oscillator based asynchronous controller

Once the internal low voltage bus gets charged to its threshold setting, e.g. 1 V, the comparator in the 2nd stage (Fig. 1) trips, activating the corresponding pulse generator. The controller building block is fully asynchronous. Control modules for different renewable sources vary in switching frequency, duty cycle, and are phase mismatched with each other. Capacitors and reference resistors shown in Figs. 1 and 2 can all be built using devices in a fully integrated CMOS design. Programmability should be added to the threshold circuits. Similarly, the oscillator load capacitors can be tunable for base frequency adjustments.

3. BOOST CONVERTER

3.1 Requirements

The next consideration is the boost converter topology selection and design for the TE sources. Utilized figures of merit for the evaluation were:

$$I-O \text{ Efficiency} = \frac{\text{Output Power}}{\text{Total Input Power}} \quad (2)$$

$$\text{Generation Surplus} = \text{Output Power} - \text{Consumed PE Power} \quad (3)$$

Input-to-Output (I-O) Efficiency tracks generated power against the power from the TE module plus any additional power delivered to the power electronics. *Generation Surplus* must be larger than 0 for a particular boost converter design to benefit. PE in the surplus equation denotes power electronics. Because the *generation surplus* is as important in sustainable power management as the *I-O efficiency*, the asynchronous controller works well for the application. As long as current is blocked, via a diode stage, from flowing into the

boost circuit from the high-V bus, net output power from regulator and controller is guaranteed to be positive. Thus, only the additional circuits, such as added comparators and voltage dividers in Fig. 1, need to be managed for power consumption to ensure a positive *generation surplus*.

3.2 Design

Various schemes for boosting up the low voltage levels were analyzed with the above metrics:

i) *Two stage conventional boost*: Both stages (Fig. 3) operate in discontinuous conduction regime with the asynchronous controller. This is a well understood configuration, but has the disadvantage of having magnetic components that are typically hard to integrate. In addition, the losses through the inductors, diodes, and switching transistors are significant. The circuit was simulated using 90nm CMOS technology to form a baseline for comparison against the other topologies.

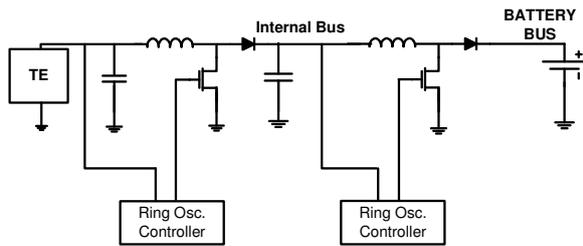


Fig. 3: Two stage conventional boost

ii) *Conventional boost – Dickson charge pump cascade*: The Dickson style charge pump is described in [5]. It should suffice to note for our purposes that a Dickson pump with T stages has an approximate output voltage of:

$$V_{out} = \sum_{N=1}^T (V_{in} - V_t(N)) \quad (4)$$

where $V_t(N)$ is the MOSFET threshold voltage at stage N. With ground body bias, source to bulk voltage increases at later stages of the Dickson pump, which in turn increases V_b , and diminishes returns for the added stages. Furthermore, when low V_{in} is used to power the pulse generator to the pump, gain significantly reduces, and impacts the I-O efficiency of the first stage. The circuit structure with only the second stage replaced by the charge pump is hence depicted in Fig. 4.

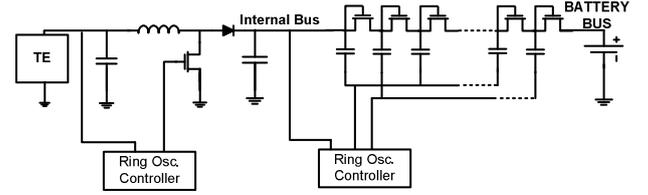


Fig. 4: Conventional boost – Dickson charge pump cascade

iii) *Low-Voltage CMOS – Dickson charge pump cascade*: A more suitable circuit for the first stage is the Low-Voltage CMOS charge pump implementation reported in [6]. This implementation is based on a cross-connected NMOS input pair followed by a PMOS output pair to ensure a voltage step-up by $V = V_{in}$ at each stage. The complete topology, with the low transistor count Dickson charge-pump at the second stage, is shown in Fig. 5. The operation details of the Low-V CMOS pump will not be described here, and can be found in [6]. It suffices to note that for the 4 stage charge pump, the ideal output voltage is 5 ($N+1$) times V_{in} . Therefore, with an internal bus of 1 V, a V_{in} level as low as $\sim 250\text{mV}$ is supported by the four stages, including the parasitic losses.

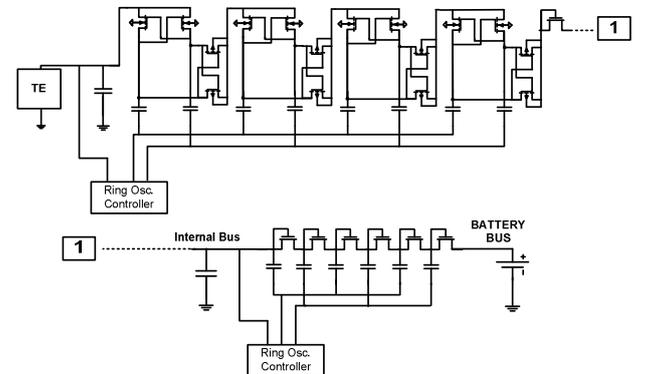


Fig. 5: Low-V CMOS – Dickson charge pump cascade

Switch capacitors [7] require many switch transistors and caps, and have large associated losses based on preliminary studies. They also require significant redundancy when the source voltage has a large operating range. Therefore, they are not further discussed in this paper.

4. RESULTS

Comparative simulations performed in 90nm CMOS technology with 1 V internal bus value

demonstrate (Table 2) the superior performance of the cascade with integrated Low-V CMOS charge pump. The poor performance of the Dickson charge pump when placed in the first stage, and the large comparative losses in the conventional boost are also shown in the same table.

1st Stage Boost Converter	2nd Stage Boost Converter	Source P (mW)	1st Stage Gen. P (mW)	2nd Stage Gen. P (mW)	Generation Surplus (mW)	Input-Output Efficiency
Conventional	Conventional	9.1	4.7	2.0	2.0	22%
Conventional	Dickson Charge Pump	9.0	4.5	3.4	3.4	37%
Dickson Charge Pump	Dickson Charge Pump	10.0	3.1	2.3	2.3	23%
CMOS Low-V Charge Pump	Dickson Charge Pump	9.4	5.5	4.1	4.1	44%

Table 2: Boost scheme comparisons for a bulk micro-TE module with 30 C ΔT across: Input 250mW at the TE; Output 6 V DC (battery) bus

Simulations, though not shown here, have indicated that, unlike the charge pumps, conventional boost I-O efficiency suffers significantly from low voltage due to the fact that I_{ds} reduction in the MOSFET is dominant over the reduction in gate switching losses. This was also demonstrated in a fast prototype with discrete MOSFET, diode, capacitor, inductor, comparator, and timer components. The conventional boost did not work at TE voltages. The charge pump scaled nicely (Table 3) to lower voltages, and had a positive generation surplus even with bulk components.

1st Stage Boost Converter	2nd Stage Boost Converter	Source Power (mW)	Output Power (mW)	PE Consumed Power (mW)	Generation Surplus (mW)	Input-Output Efficiency
Conventional (6 V)	Conventional (6 V)	0.3	0.1	7.2	-7.100	1%
Dixon Charge Pump (6 V)	Dixon Charge Pump (6 V)	8.8	26.4	75.6	-49.2	26%
Dixon Charge Pump (1 V)	Dixon Charge Pump (1 V)	4.5	8.0	6.0	2.0	57%

Table 3: Measured TE generation efficiency trends for boost scheme and supply voltage

5. CONCLUSION

The requirements and evaluation metrics have been defined in this work for low voltage, low power energy scavenging applications such as

thermoelectric generation in computing systems. A ring oscillator controlled asynchronous charge pump has been designed by taking advantage of simple building blocks to effectively address the application requirements. It has been shown through simulations using 90nm CMOS technology that close to 50% I-O efficiency and net power benefits (generation surplus) can be achieved using Low-V CMOS and Dickson charge pump topology even with a high overall step up ratio of 20. Since the circuits do not contain magnetic components, they are suitable for LSI integration, and scale well with process and voltage.

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