Generic Scheme for Designing an Adaptive Load Input Matching Charge Pump

D. Maurath[1], M. Ortmanns[1], Y. Manoli[1,2]
[1]Chair of Microelectronics, Department of Microsystems Engineering (IMTEK), University Freiburg, Germany
[2]HSG-IMIT – Institute for Micromachining and Information Technology, Villingen-Schwenningen, Germany

Abstract: This paper presents a generic scheme for designing a charge pump converter for micro-generator interfacing. This interface is able to provide adaptive load matching for achieving maximized generator power. Different topologies are presented which use the basic principle of applying oversampling capacitors to an inductive micro-generator. The paper explains a detailed method for designing and implementing such converters.

Key Words: generator interface, impedance matching, energy harvesting, conversion efficiency

1. INTRODUCTION

Due to the large and significant source impedance Z_{gen} of micro-generators (Fig. 1), matching of the applied load is essential for harvesting maximum power [1,2]. Due to mostly unpredictable transient conditions of generator excitation and loading, appropriate decoupling between the generator and the load must be introduced. This allows enhanced load impedance matching. Thus, instead of a simple blocking capacitor after the rectifier, an interface, which adaptively self-adjusts its equivalent input resistance, is mandatory [2].

In order to be able to implement such an adaptive and load matching interface that works not only for specially designed micro-generators, a general design methodology for such interfaces is desired. Improvements regarding less chip-area, higher voltage conversion ratios (c_{ratio}) as well as less switching and control losses are further design issues.

The theory and design basics are given in Section 2. Different charge pump topologies and the related trade-offs are presented in Section 3. A specific design example for an inductive as well as a piezoelectric generator is given in Section 4. Simulation results are given in Section 5 and Section 6 concludes this paper.

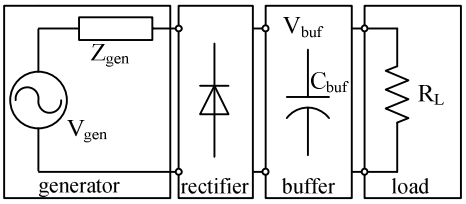

Fig. 1: Simplified Energy-harvesting system.

2. DESIGN APPROACH BASICS

Load matching can be reasonably increased by applying switched capacitors with controlled charging states [1]. Since in energy harvesting applications, the generator excitation frequencies f_{gen} are usually relatively low – some 100 Hz at most – oversampling can be easily obtained. That means, the generator output voltage waveform V_{gen} is sectioned in many time slots, as depicted in Fig. 2. Provided that each time slot Δt_i is short enough it can be assumed to have a constant instantaneous open circuit generator voltage $V_i = V_{gen}(t_i)$ within a single time slot Δt_i (Figs. 2 and 3).

For obtaining the highest possible generator output power the switched capacitors need to be charged only within a tiny voltage window around ½ V_i, as illustrated in Fig. 3 [1,3]. The peak power $P_{gen,max,i}$ exactly equals the possible maximum power, which corresponds to the impedance matching condition. Therefore, the voltage of a switched capacitor is increased by

$$\Delta V_C = (k_{stop} - k_{start})\ V_i = \Delta k\ V_i = 2\ \varepsilon\ V_i \qquad (1)$$

within a single time slot. Thereby, $k_{start} = ½ - \varepsilon$ and $k_{stop} = ½ + \varepsilon$, with $\varepsilon \to 0$ for maximum impedance matching. Hence, in each time slot the input capacitor is charged from $V_{start} = k_{start}\ V_i$ to $V_{stop} = k_{stop}\ V_i$.

A further issue is that generator current flow should be sustained even though the buffer voltage V_{buf} might be higher then V_i. Thus, generator output power could be harvested independently of V_{buf}. In order to achieve this, the voltage V_{stop} needs to be converted up to V_{buf}. As listed in Tables 1 and 2 a reasonably high load matching is obtained with ε = 0.05 and a phase angle range of

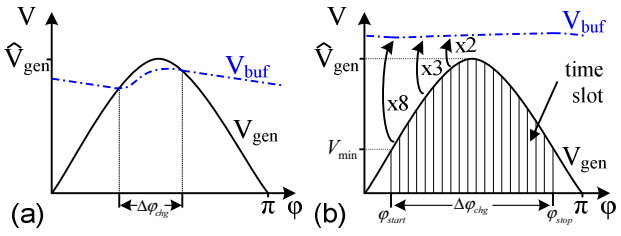

Fig. 2: Harvesting with common buffered rectifier (a) is compared to the oversampling interface (b).

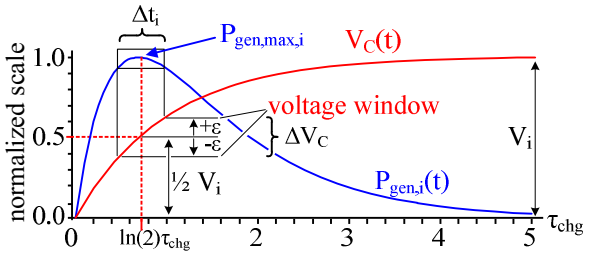

Fig. 3: Normalized capacitance charging curve $V_C(t)$ with constant V_i is plotted. The voltage window is located around ½ V_i for approaching peak power transfer.

$30° \leq \varphi_{start} << \varphi_{stop} \leq 150°$. Thereby, the instantaneous generator output power $P_{gen,i}$ is related to the theoretically maximum possible generator power P_{max}. Thus, the performance of load matching is calculated with

$$\eta_{in,i} = \frac{P_{gen,i}}{P_{max,i}} = \frac{1}{T_{ch}} \frac{\int_{t_{start}}^{t_{stop}} V_i I_i dt}{V_i^2 / (4R_{gen})} . \quad (2)$$

Thereby, t_{start} and t_{stop} correspond to V_{start} and V_{stop}.

In order to estimate the necessary switching frequency f_{switch} and switching capacitor size C_{in}, further parameters need to be defined in addition to Δk, c_{ratio} and $V_{gen,min}$, by considering worst-case conditions. These parameters are the maximum expected generator open-circuit peak-voltage $\hat{V}_{gen,oc}$, the maximum generator frequency f_{gen} and the minimum affordable delay time t_d of the switching electronics. For guaranteeing reliable oversampling, $\Delta V_{i,max}$ is additionally defined, which describes the maximum allowed generator voltage change within Δt_i. Thus, $\Delta t_{i,max}$ can be calculated with

$$\Delta t_{i,max} = \frac{\Delta V_{i,max}}{\omega_{gen} \hat{V}_{gen,oc}} = \frac{\Delta V_{i,max}}{2\pi f_{gen} \hat{V}_{gen,oc}} . \quad (3)$$

Thereby, maximum slope point of a sine wave is considered for Eq. 3. In accordance with the generator impedance Z_{gen}, which is simplified to $R_{gen} \approx Z_{gen}$ here, the maximum possible switch capacitance is given by

$$C_{in,max} = -\frac{2\Delta t_{i,max}}{R_{gen} \ln\left(\frac{1-\Delta k}{1+\Delta k}\right)} = \frac{K}{\hat{V}_{gen,oc} R_{gen} f_{gen}} . \quad (4)$$

Whereas the charging time T_{ch} of C_{in} from V_{start} to V_{stop} is given by

$$t_{start} = -\tau_{chg} \ln\left(1 + \frac{V_{start}}{V_i}\right) = -\tau_{chg} \ln\left(\frac{1}{2} + \Delta k\right) \quad (5)$$

$$t_{stop} = -\tau_{chg} \ln\left(1 - \frac{V_{stop}}{V_i}\right) = -\tau_{chg} \ln\left(\frac{1}{2} - \Delta k\right) \quad (6)$$

$$T_{ch} = t_{stop} - t_{start} = -\tau_{chg} \ln\left(\frac{1-\Delta k}{1+\Delta k}\right) . \quad (7)$$

Due to the commonly high generator source resistance R_{gen}, all other series resistances are negligible and, hence, the time constant is calculated by $\tau_{chg} \approx R_{gen} C_{in}$. With Eqs. (3) and (4) design parameter K is calculated as

$$K = -\Delta V_{i,max} \frac{1}{\pi \ln\left(\frac{1-\Delta k}{1+\Delta k}\right)} . \quad (8)$$

Thus, for a certain generator with maximum voltage $\hat{V}_{gen,oc}$ and for a certain $\Delta V_{i,max}$ maximum possible generator frequency is limited to

$$f_{gen} \leq \frac{\Delta V_{i,max}}{\hat{V}_{gen,oc} R_{gen} C_{in}} \times \frac{1}{\pi \ln\left(\frac{1-\Delta k}{1+\Delta k}\right)} . \quad (9)$$

Final calculation of an optimized switch capacitance value may need several iterations since many design parameters and trade offs are available. Regarding integrated circuit design, there are at least 4 crucial design constraints. First, a minimum t_d, which should be higher than $t_{d,min} \geq 1\mu s$ for low power operation. Second, a process dependent maximum allowed voltage might limit $\hat{V}_{gen,oc}$. Transistor threshold voltages and dynamic power losses define a third constraint parameter of limited $V_{gen,min}$. Finally, available and affordable chip area is mostly also a constraint. In accordance to those restrictions, main design objectives are (1) minimizing the dynamic power loss and chip area as well as (2) minimizing Δk and maximizing c_{ratio} for best possible power harvesting. From the equations given above, basic proportionalities can easily be extracted and applied to designs, like in Section 4.

Table 1: Parameters and corresponding ΔV_C.

ε	$P_{gen,i}/P_{max,i}$	$V_i = 0.5$ V	$V_i = 2$ V
0.05	0.98	$\Delta V_C = 0.05$ V	$\Delta V_C = 0.2$ V
0.1	0.944	$\Delta V_C = 0.10$ V	$\Delta V_C = 0.4$ V
0.15	0.87	$\Delta V_C = 0.15$ V	$\Delta V_C = 0.6$ V

Table 2: Examples of maximum charging times T_{ch}.

R_{gen}	f_{gen}	$\hat{V}_{oc,max}$	$T_{ch}=\Delta t_{i,max}$	$C_{in,max}$
500 Ω	100 Hz	3 V	5.3 µs	25 nF
5 kΩ	100 Hz	3 V	5.3 µs	2.5 nF
100 kΩ	150 Hz	5 V	3.2µs	50 pF

3. DESIGN TOPOLOGIES

For realizing a high efficient operation over a wide range of generator parameters, several charge pump topologies are necessary. Two topologies, parallel-stack as well as multistep conversion, are discussed in detail.

3.1 Parallel-Stack Conversion

In this topology after each time slot Δt_i two capacitor arrays are complementarily toggled between the charging state S_c and the transfer state S_t. At S_c, capacitors of an array are connected parallel to the generator and charged to V_{stop}. Contrary, at S_t the array capacitors are stacked in series so as to up-convert V_{stop} and exceed the output buffer voltage level V_{buf}. Hence, previously harvested charge is transferred to the output buffer C_{buf}.

The advantage of this topology is the relatively simple realization and voltage control. However, for reasonable conversion ratios c_{ratio} in conjunction with the lowest possible switching frequencies a contradiction arises between affordable on-chip capacitance (area) and switching losses as well as conduction losses. Usually, with standard CMOS processes not more than 1.5…2 nF/ mm^2 is possible. Locating many capacitors off-chip is usually not feasible. For reasonably small $\Delta k = 0.05…0.1$ and $\Delta\varphi_{chg} \rightarrow 120°$ at least a factor of $c_{ratio} = 4$ is necessary. Hence, for two arrays, at least 14 pins and a huge circuit board footprint is required.

3.2 Multistep Conversion

With multistep conversion, realizing a switching converter with less capacitors becomes possible [4]. This new approach provides higher c_{ratio} and, due to fewer required capacitors, the possibility of off-chip capacitors saves large chip area. Instead of 2x6 capacitors for $c_{ratio} = 6$ in the parallel-stack approach, only 5 capacitors are necessary for obtaining $c_{ratio} = 8$. This novel approach employs three peripheral capacitors $C_{P1…3}$, which could easily be located off-chip and two stacking capacitors $C_{S4…5}$. $C_{P1…3}$ are connected to the generator in a cyclical order. Thus, during a charging phase only one capacitor is connected to the generator and charged to V_{stop}. At the same time, the other two peripheral capacitors are stacked together to provide a voltage which is double the V_{stop} of the previous charging phase. These stacked capacitors propagate charge to the capacitors $C_{S4..5}$ and buffer C_{buf} in an adaptive configuration depending on the necessary c_{ratio}. As illustrated in Fig. 4, the two stacked peripheral capacitors charge C_{S4} and C_{S5} to a voltage which is the sum of both V_{stop} of the two previous charging phases. In the next charging phase, the next peripheral capacitor (C_{P2}) is connected to the generator and the previously charged C_{P1} is now connected parallel to C_{P3}. If then C_{S4}, which was previously charged to a voltage of twice V_{stop}, is stacked on top of C_{P1} and C_{P3} a stack voltage of three times V_{stop} is generated. A factor of $c_{ratio} = 7$ is obtained, if this principle of subsequent stacking in conjunction with the cyclical connection of the peripheral capacitors to the generator is consequently repeated.

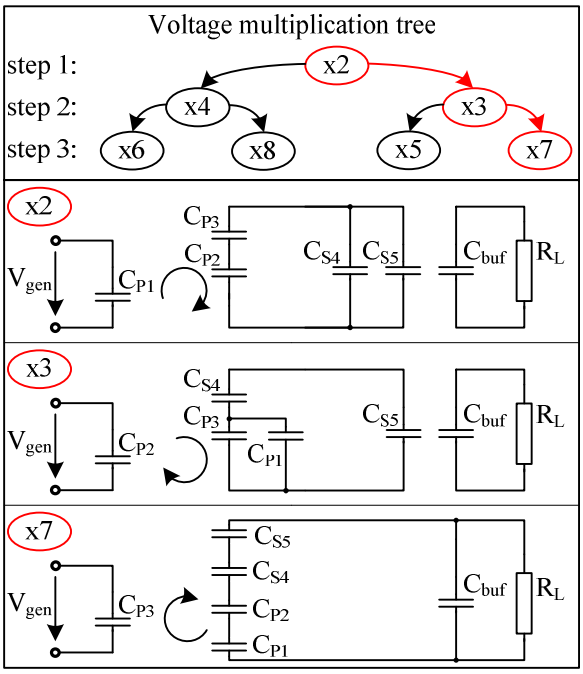

Fig. 4: Voltage conversion tree and multi-step conversion is exemplary shown for $c_{ratio} = 7$.

For preserving impedance matching conditions it is important to operate the peripheral capacitors within an appropriate voltage window around ½ V_i. Therefore, the same comparator based control as used for the parallel-stack topology is possible. For controlling the charging states of the stacking capacitors two further comparators as well as switching logic needs to be implemented.

3.3 Topology Selection Criteria

Since harvesting generators vary in principle and performance only general considerations can be given here. The necessary capacitance C_{in} strongly depends on parameters R_{gen} ,f_{gen}, and $\hat{V}_{gen,oc}$, as Eq. 9 expresses. The relation of these parameters defines the available generator power - often some 100 µW.

Therefore, using on-chip capacitors is only reasonable if a capacitance of not more than around 5 nF is possible. Otherwise, the multistep approach is preferable. The only restriction to the multistep approach is that the generator amplitudes and load transients should be quite constant in order to simplify the control of the charging states of the multistep converter.

4. GENERATOR RELATED DESIGN

Usually, a generator is electrically defined by its equivalent internal resistance R_{gen}, the expected maximum open circuit output voltage $\hat{V}_{gen,oc}$ and a frequency f_{gen}. For paying attention to reliable operation

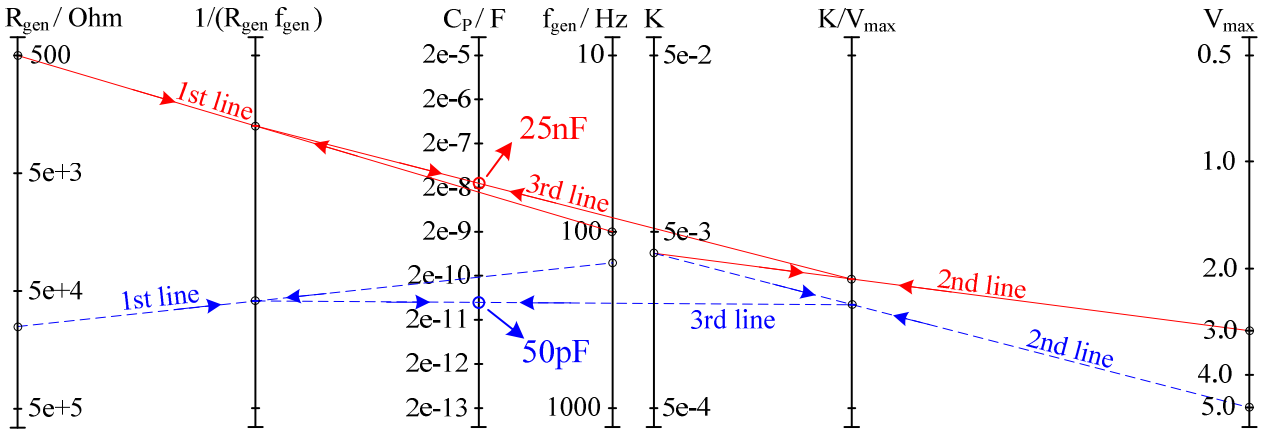

Fig. 5: Nomogram relating R_{gen} -- f_{gen} to a 1st and K – $V_{gen,oc}$ (V_{max}) to a 2nd auxiliary point. Connecting both auxiliary points results in the necessary converter input capacitance C_{in} (K = 3.756E-03). The dashed blue lines show a piezo-generator example and the red lines give an example for a typical inductive generator.

and optimized performance of the electronics, a design parameter K is used. This is done by considering worst case conditions with respect to sufficient oversampling, ability of adaptive charging and necessary c_{ratio}. The nomogram in Fig. 5 and Table 3 relates these parameters for specifying the necessary C_{in}.

Table 3: Parameters for Fig. 5 are provided.

	V_{max}	R_{gen}	f_{gen}
piezo	5V	100 kΩ	150Hz
inductive	3V	500 Ω	100 Hz

K	Voltage window: 0.6...0.8 τ_{chg} Conduction angle $\Delta\varphi_{chg}=2\alpha$: 120° $\Delta V_{i,max}$ at a time slot: 10mV	3.756E-03

5. SIMULATION RESULTS

Simulation results are obtained with a Spectre circuit simulator and given in Fig. 6. The fundamental difference of achievable power is obvious for light-load as well as heavy-load conditions when compared to a traditional full-wave rectifier with blocking capacitor η_{common}. These light and heavy load conditions can be related for example to a sleep period and to wireless transmitting activity of an autonomous sensor node.

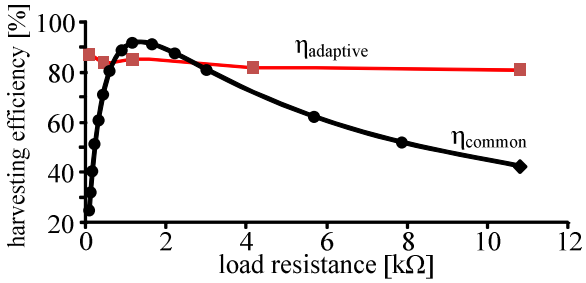

Fig. 6: Comparison of harvesting efficiencies based on the inductive generator of Fig. 5.

6. CONCLUSION

Basic design relations are presented for implementing charge pump based generator interfaces with improved impedance matching. Useful considerations lead to simplification and inclusion of all important design parameters into a single equation. This gives designers of such interfaces an easy and fast tool for calculating a concrete system. In addition, it helps to concentrate on all important design parameters, thus resulting in better optimized interfaces and easier reusability. Furthermore, a new charge pump topology was introduced and compared to a standard structure.

ACKNOWLEDGMENT

This work is supported by the German Research Foundation (Deutsche Forschungsgemeinschaft - DFG) under Grant Number GR1322.

REFERENCES

[1] D. Maurath, M. Ortmanns and Y. Manoli,"Adaptive Power Extraction from Micro Generators with Implicit Voltage Up-Conversion", PowerMEMS 2007, Volume 7, 2007, pp. 351-354.

[2] N.G. Stephen, "On energy harvesting from ambient vibration," Journal of Sound and Vibration, Volume 293, Issues 1-2, 30 May 2006, pp. 409-425

[3] D. Maurath, M. Ortmanns and Y. Manoli, "High Efficiency, Low-Voltage and Self-Adjusting Charge Pump with Enhanced Impedance Matching", IEEE MWSCAS 2008, Knoxville, USA, pp. 189-192.

[4] M. S. Makovsiki and D. Maksimovic, “Performance Limits of Switched-Capacitor DC-DC Converters”, Proc. IEEE Power Electronics Specialists Conference, pp.1215-1221, 1995