FABRICATION OF THROUGH-CHIP POROUS Pd LAYER ON Si SUBSTRATE FOR MINIATURE FUEL CELLS

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Abstract: A novel technique for fabricating through-chip porous palladium layer on the silicon substrate was developed. We are studying formation of the porous metallic layer on the silicon substrate, and developing miniature fuel cell electrodes that use the porous metallic layer as a catalyst layer. In this works, the porous palladium layer obtained by using the organic palladium complex with ethylenediamine for a porous metallic layer was used. Plasma etching was performed from the opposite side of the porous palladium layer to make fuel channels, and the through-chip porous palladium layer was successfully fabricated.

Key words: through-chip, miniature fuel cell, porous palladium layer, organic palladium complex, plasma etching

1. INTRODUCTION

High performance electric power sources are requested along with widespread use of portable electronic devices. At this point, Li ion batteries are widely used as the power source in the portable devices. However, those batteries need charging, which interrupts continuous portable use of the devices. Besides, it is becoming difficult for the batteries to satisfy storage capacity requested by increasing power consumption with the advance of the device function and performance. Then, miniature fuel cells have been studied actively by various groups. For practical use, production cost and mass productivity are important and MEMS techniques are promising for the fuel cell miniaturization because of the good mass productivity. Therefore, various studies using Si substrate and MEMS techniques have been performed [1-10]. Recently, we employed a novel catalyst layer fabrication process, in which porous Pt layer was formed on a Si substrate by using anodized porous Si as a base material[11], and fuel cell electrodes were produced monolithically with Si substrates [12].

Figure 1 shows the design of our thin fuel cell using the Si electrodes. In this design, 100μm thick Si substrate is used. It is widely known that crystalline Si becomes porous by anodization in a solution containing HF. We discovered that immersion of the porous Si to a Pt plating bath containing HF results in a complete replacement of Si to Pt and relatively thick porous Pt layer can be easily formed on Si substrates. The porous Pt layer can be used as a catalyst layer, then fuel channels are formed by plasma etching on the opposite side on the Si substrate and monolithic fuel cell electrodes are realized. Our prototype had only 230μm in thickness and showed relatively high power output among MEMS based fuel cells [12]. In the prototype, porous Pt was used as the catalyst layer and the amount of Pt usage is high. It is desirable that porous conductive layer is formed with inexpensive materials compared to Pt and the conductive layer can be used as Pt catalyst support. In this study, Pd layer is treated because of its corrosion resistance, high conductivity and catalyst activity. Porous Pd formation and its application to our monolithic fuel cell structure are attempted.

2. POROUS PALLADIUM FORMATION

The silicon wafers used in this work were n-type, 0.001-0.005Ωcm resistive, 500μm thick, (100)-oriented and mirror-polished on one side. At first, oxide layer on the wafer was removed by HF solution. Then, mirror-polished side is anodized in an electrolyte containing HF using a homemade fluorocarbon polymer vessel. In the anodization process, electric current is applied on the back side of the wafer through contact pins. Then, anodization electrolyte is removed from the vessel and a dilute

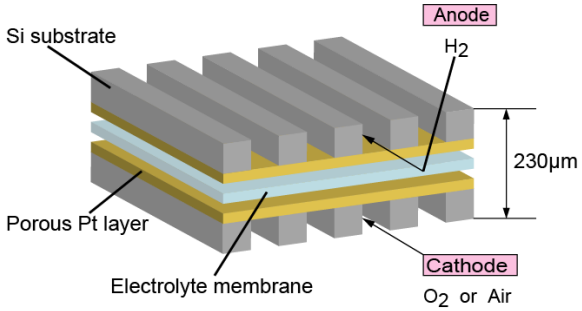

Fig.1: Schematic view of the Si based fuel cell

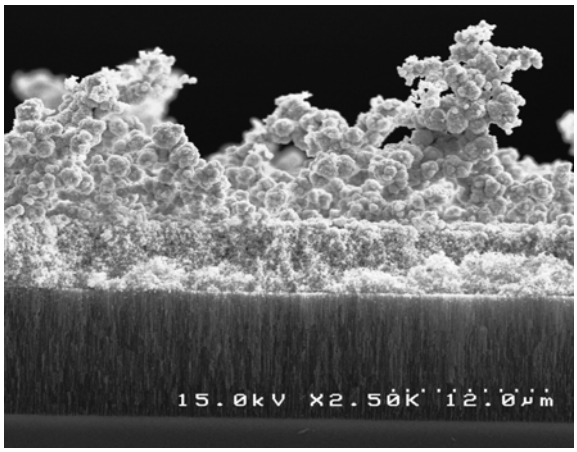

Fig.2: The cross-sectional view of porous Pd layer using $PdCl_2$ plating bath

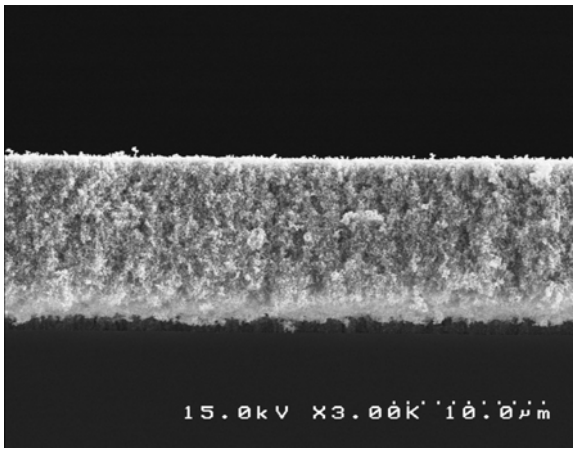

Fig.3: The cross-sectional view of porous Pd layer using ethylenediamine complexation bath

Table 1: Condition of porous Pd formation

Pd ion	**$[PdCl_4]^{2-}$**	**$[Pd(en)_2]^{2+}$**
Property of Si substrate		
Crystal Orientation	(100)	
Type	N	
Thickness of Si substrate	500µm	
Resistivity [Ωcm]	0.001-0.005	
Anodization condition		
Composition of solution	Water:HF(46%):Ethanol=5:3:2	
Current density [mA/cm^2]	60	
Time [sec]	450	
Alkali etching condition		
Composition of solution	20mM NaOH	
Time [sec]	60	
Immesion plating condition		
Composition of plating bath	20mM $PdCl_2$	20mM $PdCl_2$
	60mM NaCl	50mM EDA
	300mM HF	300mM HF
Time [min]	20	

NaOH solution is poured into the vessel. It is known that anodized porous Si layer has a micropore layer in the vicinity on the top surface and the micropore layer tends to form dense metal film during the immersion plating. Therefore, the micropore layer is removed by the NaOH etching. Finally, 20mM Pd ion containing plating solution is poured into the vessel and strong agitation is applied. The plating solution contains fluoride ion. In the plating bath, Pd ion is reduced and deposited on Si and Si oxidizes. Oxidized Si can be dissolved with fluoride ion and porous Si is replaced to Pd. All experiments are performed in a temperature controllable chamber at 283K. The specimen chip is cleaved and SEM observation is performed.

2.1 $PdCl_2$ plating bath

Anodization and plating conditions are listed in table 1. $PdCl_2$ was used as Pd ion source. Because $PdCl_2$ is insoluble in pure water, $PdCl_2$ was dissolved in NaCl solution. Then, HF solution was neutralized to pH 3 by adding NaOH. Concentrations of Pd ion and fluoride were tuned to 20mM and 300mM respectively. Neutralization was performed for comparison to experiments with following organic complexation described in section 2.2. Cross sectional image of the porous layer is shown in figure 2. About 5µm thick porous Pd layer was obtained, though there were large columnar deposits. By elemental analysis by EDS (Energy Dispersive Spectroscopy), those columnar product was Pd. The surface seems to be too rough for our fuel cell design to be applied. The irregular deposit might be caused by rapid growth of the deposit and suppression of the deposit growth was considered.

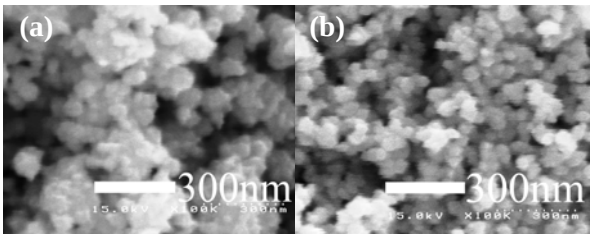

Fig.4: Comparing the particle of Pd. (a) Using $PdCl_2$ bath, (b) Using ethylenediamine complexation bath

2.2 Ethylenediamine complexation bath

In order to suppress deposition rate, there are several ways, such as additives and ion complexation [13, 14]. Additives are usually assumed that they adsorb and form inhibition layer on the plating surface, while ion complexation controls electrode potential. In this case, surface condition is complex because the surface composition changes from Si to Pd during the plating process and it may cause difficulties to control surface conditions. In our

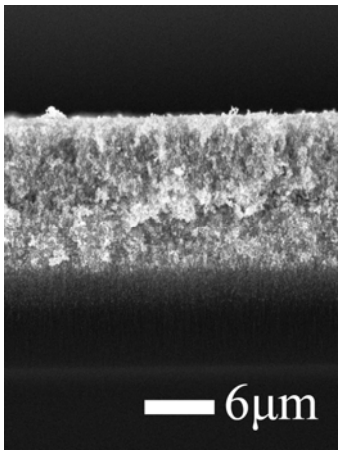

Fig.5: The cross-sectional view of porous Pd layer

Table 2: Condition for through-chip porous Pd

Pd ion	**$[Pd(en)_2]^{2+}$**
Property of Si substrate	
Crystal Orientation	(100)
Type	N
Thickness of Si substrate	100μm
Resistivity [Ωcm]	0.004-0.006
Anodization condition	
Composition of solution	Water:HF(46%):Ethanol=5:3:2
Current density [mA/cm^2]	90 → 0
Time [s]	620
Alkali etching condition	
Composition of solution	20mM NaOH
Time [sec]	60
Immesion plating condition	
Composition of plating bath	20mM $PdCl_2$
	50mM EDA
	450mM HF

previous study, porous Au was successfully obtained with ethylenediamine complexation of Au ion [15]. Therefore, we tried complexation and ethylenediamine was employed in this experiment. PdCl2 and ethylenediamine were used for forming Pd complexed ion. Pd(II) has 4 coordinates and ethylendiamine has 2 coordinates. Mixture of PdCl2 and ethylendiamine with one-two molar ratio would make the complex ion $[Pd(en)_2]^{2+}$, but it took long time for dissolution. Then, mixture of PdCl2 and ethylendiamine with two-five molar ratio was used for $[Pd(en)_2]^{2+}$ preparation. The $[Pd(en)_2]^{2+}$ solution was tuned to pH 3 by adding H_2SO_4. HF solution was also neutralized to pH 3 by adding NaOH and the $[Pd(en)_2]^{2+}$ solution was mixed with the HF soultion. Concentrations of Pd ion and fluoride were tuned to 20mM and 300mM respectively. Below pH 3, $[Pd(en)_2]^{2+}$ becomes instable and pH 3 was used in the experiments. Cross sectional image of the porous layer is shown in figure 3. It was found that the large columnar deposits were successfully suppressed and

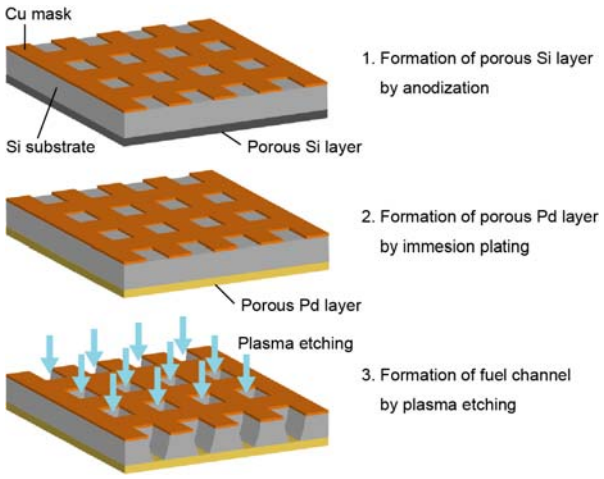

Fig.6: Fabrication process of the monolithi electrode.

11μm thick porous Pd layer was obtained. Particle size of the deposited Pd was compared in figure 4 and smaller size was observed with the complexation.

3. THROUGH-CHIP POROUS Pd LAYER

3.1 Porous Pd layer for the electrodes

It was found that porous Pd layer can be successfully obtained by complexation of Pd ion. In order to apply the porous Pd layer, we needed to form the porous layer on a Si wafer of 100μm thick and mirror-polished on both sides. In this section, n-type and 0.004-0.006Ωcm resistivity wafer was used. Some tuning for fabrication parameter was needed and the condition shown in table 2 was employed. As shown in figure 5, 14μm thick porous Pd layer was obtained.

3.2 Fabrication of the through-chip structure

Porous Pd layer could be obtained on the 100μm thick wafer. Then the through-chip porous Pd structure for the miniature fuel cells was attempted to be made. Before the formation of porous Pd, etching mask for fuel channels was made. Thermal oxide film was removed by HF. Then, thin Cu film was deposited on one side by sputtering. The Cu film is expected to work as a plasma etching mask and a current path. Using usual photolithographic patterning with photoresist and wet Cu etching, mask for fuel channel etching was patterned with the Cu film. Procedure of the anodization and porous metallization was same as used in section 2.

Finally, plasma etching was applied from the Cu mask side. Etching machine with conventional parallel plate electrodes (Samco RIE-10N, Japan) was used. Gas composition for the etching was 18.0sccm of SF_6 and 4.0sccm of O_2 and 30W power

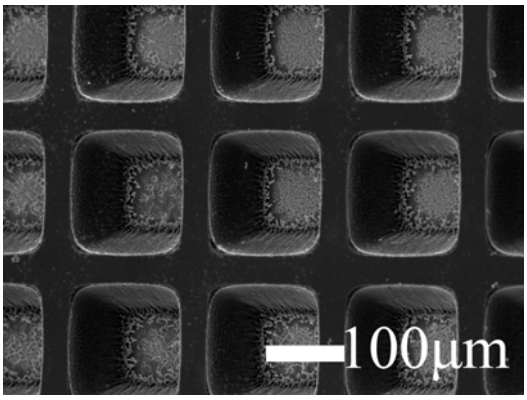

Fig.7: The view of the specimen chip

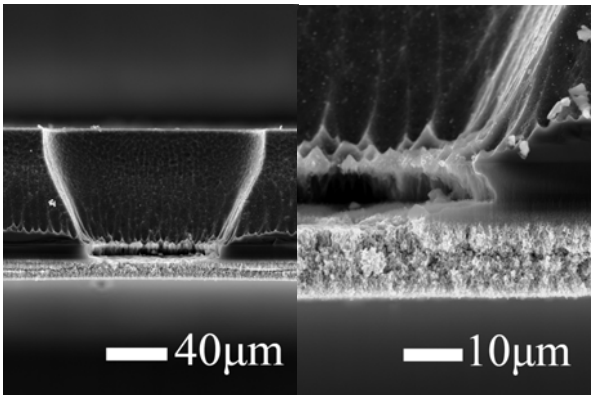

Fig.8: The cross-sectional view of the chip

was applied. Etching rate was measured by some preliminary experiments and 1.3μm/min was used for depth estimation. Then, plasma etching was performed for 68min, so that the bottom of the etched pits reached to the porous layer on the other side. Figures 7-8 shows the specimen chip after the plasma etching. It was found that the through-chip porous Pd layer was successfully fabricated and the porous Pd layer worked as a stopping layer for the plasma etching. In the case with Pt, Pt poor porous region seemed to be much resistive to plasma and worked as a stopping layer, while in the present case with Pd, Pd poor porous region was etched away. Because the region is important for fuel supply, further study will be needed to understand the different behavior.

4. CONCLUSION

Fabrication of through-chip porous Pd layer was successfully demonstrated on a Si wafer. Almost identical way as fabrication of the through-chip porous Pt layer was applicable. However, the etching behavior around the boundary between the bulk Si and porous layer was different between the Pd case and Pt case. It may relate to the deposition behavior of Pd and Pt. In Pt case, it was found that porous Si rich region was still remained. The etching rate of the Si rich region was slower than Pd case. It is supposed that the Si oxide or small amount of Pt deposition suppress the plasma etching. But it is not investigated carefully yet. Further study for the difference may be needed.

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