Through-chip porous Ru-Pt catalyst layer for miniature DMFC

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Abstract: A through-chip porous Ru-Pt catalyst layer for miniature DMFC application was fabricated on a Si wafer. Recently, we found that porous noble metal layer can be synthesized on Si substrate by immersion plating on a porous Si. In order to realize a DMFC with our novel structure, a porous Ru layer was synthesized on the Si substrate using the immersion plating on the porous Si, then Pt was deposited by galvanic replacement reaction on the porous Ru. The porous Ru-Pt structure shows catalytic activity on methanol oxidization. Fabrication of a through-chip porous Ru-Pt layer was demonstrated with identical plasma etching process used in the porous Pt study.

Key words: miniature fuel cell, DMFC, porous Si, galvanic replacement, plasma etching, MEMS

1. INTRODUCTION

Along with the development of high performance mobile electronic products, energy consumption of those equipments is increasing. At this point, improvement of Li ion battery could manage to satisfy the requirement of those electronic devices. Combustible fuels have high energy potential and methanol has 10 times higher energy density (volume) compared to present Li ion batteries for instance. Therefore, DMFCs (direct methanol fuel cell) have received much attention as ultimate portable power sources.

Recently, we found that porous Si can be completely replaced to porous Pt by immersion plating and porous Pt layer can be easily formed on Si substrates. Using the porous Pt layer as an etching stop layer in a plasma etching process, a though-chip porous Pt catalyst layer was successfully fabricated on a Si substrate. Then, we demonstrated a prototype of miniature fuel cell with the through-chip porous Pt layer, which works as a catalyst layer, and relatively high output was obtained among MEMS based fuel cells [1].

In the above miniature fuel cell study, hydrogen was used as a fuel. In order to use methanol, Ru is an essential material for the catalyst. There are some reports that catalyst consisting of Ru, on which Pt is deposited by galvanic replacement reaction, shows high catalyst reactivity [2-10]. Then, we attempted to synthesize a porous Ru layer by identical way as porous Pt formation. The porous Ru layer was successfully obtained and Pt deposition on the Ru layer was also performed. Our preliminary results showed that the porous Ru-Pt layer had catalytic activity for the methanol oxidization [12]. Therefore, it seems possible to produce a miniature DMFC with our monolithic Si electrodes design. In this study, fabrication of through-chip porous Ru-Pt layer was attempted to realize the miniature DMFC structure.

2. THROUGH-CHIP POROUS Ru-Pt LAYER FABRICATION

2.1 Miniature DMFC Design

Figure 1 shows our miniature DMFC design. Through-chip porous Ru-Pt layer monolithically formed on a Si substrate is expected to work as a catalyst layer. A PEM (Polymer Electrolyte Membrane) sheet is put between two Si electrodes. Fuel channels are formed on the Si substrate. Because the electrodes are monolithic, large clamping force is not needed and quite thin structure can be expected. Thickness of the Si substrate and PEM sheet now used

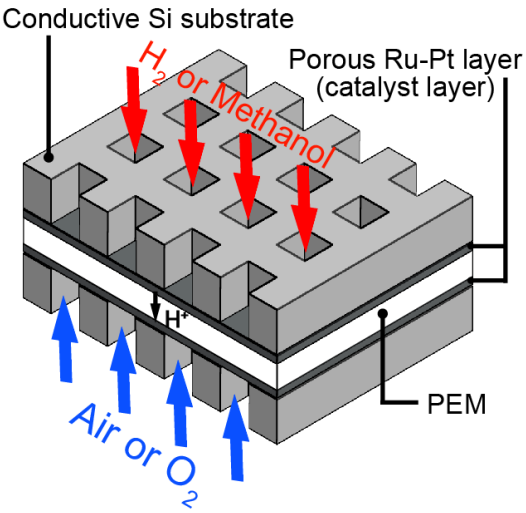

Fig. 1: Schematic view of the Si based fuel cell.

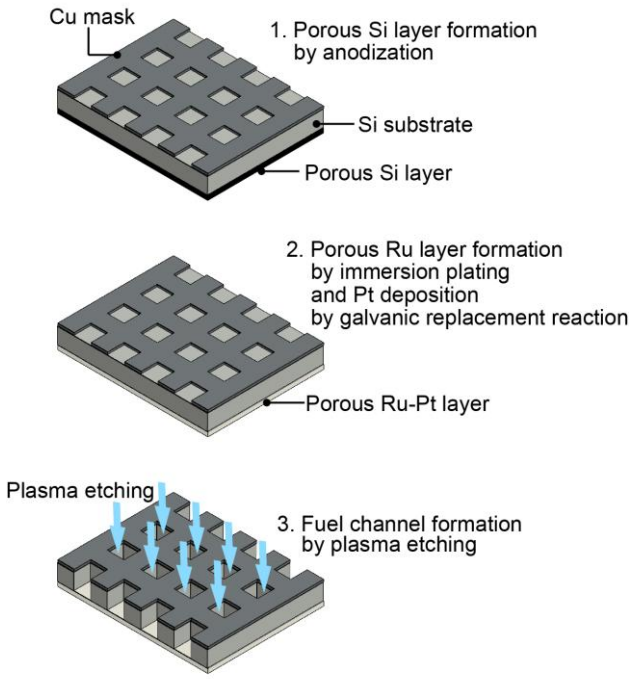

Fig. 2: Fabrication process of the monolithic electrode.

is 110μm and 15μm respectively, and the total thickness of the cell can be less than 250μm. The small thickness is advantageous for cell stacking and high output density can be expected.

2.2 Fabrication Process

Figure 2 shows a schematic view of the Si electrode fabrication process. Experimental conditions are listed in table 1. Si substrate is a 15mm × 15mm chip diced from 4inch wafer.

Copper Mask-- At first, Cu thin film is deposited by sputtering. The Cu thin film works as a electric path for the anodization process and a plasma etching mask for fuel channel formation. The Cu thin film mask is generated by usual photolithographic resist patterning and Cu wet etching with an iron dichloride solution. The mask pattern employed in this study has 3mm × 3mm square region. In this region, 100μm × 100μm square openings are made with 200μm pitch. In this study, each opening is not connected, but we need channels between each opening. The fabrication procedure for those connections is now under development.

Porous Ru-Pt Layer-- Anodization is performed in a fluorocarbon polymer vessel containing HF solution on the opposite side of the Cu mask and porous Si is formed. Anodization current is applied by contact pins to the Cu mask and a Pt wire is used as a counter electrode. After anodization, specimen chip is rinsed by acetone keeping the chip in the fluorocarbon poly-

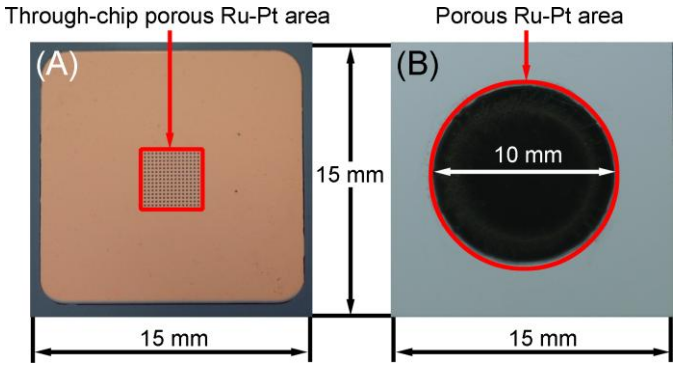

Fig. 3: Photograph of specimen chip – (A)Cu mask surface, (B)Porous Ru-Pt layer surface.

Table 1: Condition of specimen chip formation.

Property of Si substrate	
Crystal orientation	(100)
Type	N
Resistivity [Ω cm]	0.007-0.020
Anodization condition	
Composition of solution	Water : HF(46%) : Ethanol = 5 : 3 : 2 (wt)
Current density [mA/cm^2]	110
Time [s]	196.29
Ru immersion plating condition	
Composition of plating bath	1.0MH_2SO_4 + 27mM$RuCl_3$ + 400mMHF
Plating time [min]	25
Pt immersion plating condition	
Composition of plating bath	1.0MH_2SO_4 + 20mMH_2PtCl_6
Plating time [min]	20

-mer vessel. Then, immediately, Ru plating electrolyte is poured into the vessel and agitation is applied by a homemade syringe pumping equipment. Detailed instruction is described elsewhere [11]. Ru deposition is performed for 25min. During this immersion plating, Ru ion is reduced while Si is oxidized. Oxidized Si is dissolved because HF is added in the plating bath. Then, porous Ru is obtained. After Ru deposition, plating electrolyte is switched for Pt deposition. Anodization and plating process are performed in a cooled environment at 283K. After 20min of immersion, specimen chip is carefully rinsed by acetone.

Formation of Through-chip Porous Ru-Pt Layer-- Fuel channels are opened by plasma etching from the copper mask side. In this process, porous metal layer is expected to work as an etching stopping layer. This strategy was successfully verified with the porous Pt layer in our previous study [1]. Same approach is applied to the porous Ru-Pt layer. Plasma etching is applied with conventional parallel plate type etching machine (Samco RIE-10N, Japan). 18.0 sccm of SF_6 and 4.0 sccm of O_2 are fed to the chamber and 30W power is applied. Plasma etching is performed for 115min.

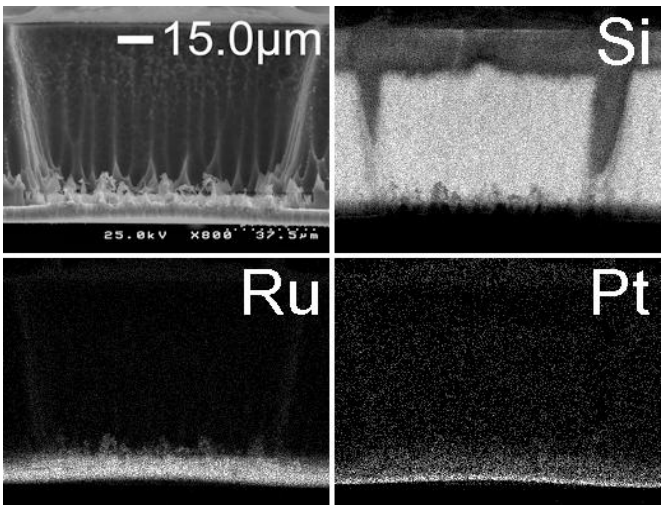

Fig. 4: Cross sectional view obtained by SEM and EDS elemental mapping of the through-chip Ru-Pt catalyst layer.

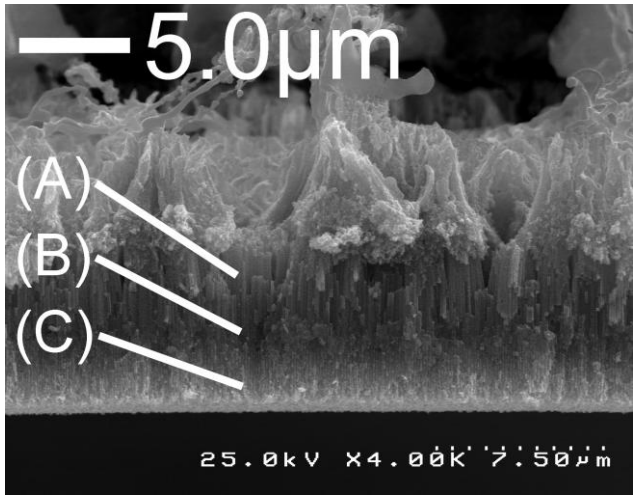

Fig. 5: Magnified view of the porous Ru-Pt catalyst layer.

Table 2: Atomic ratio of the porous layer by EDS quantitative analysis. Three points at (A), (B) and (C) in fig. 5 were measured.

	Si [At%]	Ru [At%]	Pt [At%]
(A)	16.34	79.56	4.10
(B)	4.32	87.50	8.18
(C)	3.16	72.65	24.19

3. RESULT AND DISCUSSION

Figure 3 shows specimen appearance. The dark circle in the figure 3(right) is the porous Ru-Pt layer. The specimen chip was cleaved and cross section was observed with a field emission scanning electron microscope equipped with an EDS (energy dispersive x-ray spectrum analyzer). Figure 4 shows a SEM image and elemental mappings after plasma etching. Figure 5 shows a magnified view of the porous layer cross section around the bottom of the etched opening. A result of quantitative analysis obtained by EDS is shown in table 2. Near the surface of the porous layer, residual Si signal is small and porous Ru-Pt layer can be made. It is found that the metal deposition is poor in deep area, which is close to the bottom of the etched openings. Figure 6 shows a cross sectional image of the porous Ru-Pt layer, which is synthesized by identical conditions, without plasma etching. In this figure, upside is the porous layer surface, which is opposite to the other images in figures 4-5, where downside is the original porous layer surface. In figure 5, Ru poor porous area seems shrunk and is deformed. But before plasma etching, straight pore porous feature can be seen in Ru poor porous area as shown in figure 6. In the case of porous Pt, there was also Pt poor region, but those region seemed still plasma etching resistive and smooth bottom of the etched opening was observed. This difference might relate to the deposition behavior such as particle sizes of the metal deposit. Anyway, it was clear that through-chip porous Ru-Pt catalyst layer could be obtained. We already reported that the Ru-Pt layer synthesized by identical way showed catalytic activities for methanol oxidization

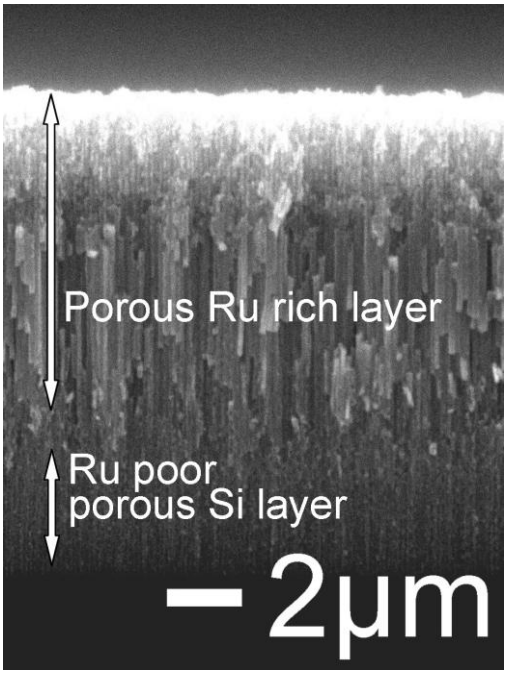

Fig. 6: Cross sectional view of the porous Ru-Pt catalyst layer.

[12] and the through-chip porous Ru-Pt layer fabrication is promising for the realization of the DMFC with our monolithic electrodes design.

4. CONCLUSION

Porous Ru rich layer was formed on a Si substrate by immersing anodized porous Si into Ru plating bath containing HF. After Ru rich porous layer formation, Pt was deposited by galvanic replacement reaction. EDS analysis showed that the porous layer contained Ru and Pt. The through-chip porous layer was fabricated by applying plasma etching from the opposite side of the porous layer. Further study for realizing miniature DMFC with the monolithic Si electrode design will be performed.

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REFERENCES

[1] T. Fujii, J. G. A. Brito-Neto, M. Hayase; Thin Si Based Fuel Cell with Porous Pt Layer Formed on a Si Substrate, *Technical Digest PowerMEMS 2007 (Freiburg, Germany, 28–29 November 2007)*, 169–172 (2007).

[2] S. R. Branković, J. McBreen, R. R. Adžić; Spontaneous deposition of Pt on the Ru(0001) surface, *Journal of Electroanalytical Chemistry*, **503** 99–104 (2001).

[3] S. R. Branković, J. X. Wang, R. R. Adžić; Pt Submonolayers on Ru Nanoparticles, *Electrochemical and Solid-State Letters*, **4**(12) A217–A220 (2001).

[4] S. R. Branković, J. X. Wang, R. R. Adžić; New methods of controlled monolayer–to–multilayer deposition of Pt for designing electrocatalysts at an atomic level, *J. Serb. Chem. Soc.*, **66**(11 –12) 887 – 898 (2001).

[5] S. R. Branković, J. X. Wang, Y. Zhu, R. Sabatini, J. McBreen, R. R. Adžić; Electrosorption and catalytic properties of bare and Pt modified single crystal and nanostructured Ru surfaces, *Journal of Electroanalytical Chemistry*, **524–525** 231–241 (2002).

[6] J. X. Wang, S. R. Branković, Y. Zhu, J. C. Hanson, R. R. Adžić; Kinetic Characterization of PtRu Fuel Cell Anode Catalysts Made by Spontaneous Pt Deposition on Ru Nanoparticles, *Journal of The Electrochemical Society*, **150** A1108–A1117 (2003).

[7] K. Sasaki, Y. Mo, J. X. Wang, M. Balasubramanian, F. Uribe, J. McBreen, R.R. Adžić; Pt submonolayers on metal nanoparticles – novel electrocatalysts for H_2 oxidation and O_2 reduction, *Electrochimica Acta*, **48** 3841–3849 (2003).

[8] K. Sasaki, J. X. Wang, M. Balasubramanian, J. McBreen, F. Uribe, R. R. Adžić; Ultra-low platinum content fuel cell anode electrocatalyst with a long-term performance stability, *Electrochimica Acta*, **49** 3873–3877 (2004).

[9] J. Zhang, M. B. Vukmirović, K. Sasaki, F. Uribe R. R. Adžić; Platinum monolayer electrocatalysts for oxygen reduction: effect of substrates, and long-term stability, *J. Serb. Chem. Soc.*, **70**(3) 513 – 525 (2005).

[10] M. B. Vukmirović, J. Zhang, K. Sasaki, A. U. Nilekar, F. Uribe, M. Mavrikakis, R. R. Adžić; Platinum monolayer electrocatalysts for oxygen reduction, *Electrochimica Acta*, **52** 2257 – 2263 (2007).

[11] J. G. A. Brito-Neto, S. Araki, M. Hayase; Synthesis and Characterization of Porous Platinum Layers Deposited on Highly Doped n-Type Porous Silicon by Immersion Plating, *Journal of The Electrochemical Society*, **153**(11) C741–C746 (2006).

[12] J. G. A. Brito-Neto, K. Kondo, Y. Saito, M. Hayase; Formation of Porous Ruthenium Layer on Porous Silicon Template, *212th ECS Meeting Abstracts, Electrochem. Soc.*, **702** 1365 (2007).