A CMOS INTEGRATED INTERFACE FOR PIEZOELECTRIC GENERATORS

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Abstract: This paper presents a low-voltage, low-power CMOS integrated interface circuit capable of optimizing the power transfer from a piezoelectric generator (PZT) into a rechargeable battery or a large capacitor. The circuit operates with PZT voltage amplitudes from 2.4 V to 7 V and input frequencies from 50 Hz to 1000 Hz. It has been designed for a supply voltage of 2 V, but the circuit keeps operable down to 1.2 V. The switching clock is derived from the PZT frequency, resulting in low switching losses. Simulation suggests conversion efficiencies up to 80% with a total power consumption of about 1.3 µW.

Key words: Piezoelectric energy harvesting, energy management, interface circuit, power transfer

1. INTRODUCTION

Energy harvesting converts ambient energy into electrical energy which can be used to supply low-power systems like wireless sensor nodes. This is very attractive in systems where replacement of batteries is not economical either because of the difficult access or due to the large number of distributed sensor nodes [1]. Vibrations appearing e.g. in industrial machinery are one possible energy source for which several conversion mechanisms exist. The piezoelectric effect is one of these mechanisms which is well-known and simple to apply. An efficient electrical interface circuit for the piezoelectric generator (PZT) is at least as important as the proper design of the generator itself since it is capable of transferring most of the generated power into a rechargeable battery or a large capacitor. Most of these interface circuits which have been reported are built from discrete electronics [2] thus consuming lots of power or can only process low PZT voltages [3]. Since the output power of PZTs increases with higher vibration magnitudes, leading to higher PZT output voltages, it is desirable that low-power integrated circuits (ICs) are available which can operate with these voltages in the range of several volts to several ten volts [2][4].

The theory behind the presented circuit is explained in section 2. Section 3 describes the implementation of the IC. In section 4, the results are presented. The paper concludes in section 5.

2. THEORY OF OPERATION

2.1 Piezoelectric generator

A piezoelectric generator (PZT) which is driven near the resonance frequency can be modeled by the simple equivalent circuit shown in Fig. 1 [3]. An AC current source represents the vibrating piezoelectric beam, whereas the peak current I_p is proportional to the vibration amplitude. The capacitor C_p and the resistor R_p are related to the dielectric and the corresponding losses inside the PZT. In order to obtain realistic simulation results, data sheet values from a standard PZT bending generator [5] are used for the simulations. The generator values are summarized in Table 1. At given PZT parameters, a certain value for I_p directly corresponds to a PZT voltage V_p.

2.2 Interface circuit

The proposed circuit which is shown in Fig. 2 realizes the principle of synchronous charge extraction which has been reported by Lefeuvre et al. [6]. Since the PZT produces an AC voltage, a rectifier is needed. An inductor acts as a temporary energy storage which is periodically charged/discharged by three MOSFET switches S1, S2 and S3. A battery or a large capacitor, e.g. a goldcap, stores the extracted power.

The operation principle is explained on the basis of Fig. 3. In this figure, a period of the rectified voltage V_{rec} and the inductor current I_L together with the timing of the switch control signals GateS1, GateS2 and GateS3 can be seen. During phase A, all the switches are open, representing an open circuit configuration for

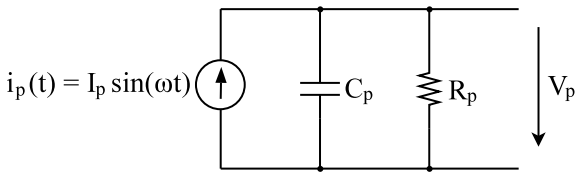

Fig. 1: Equivalent circuit of the piezo generator near the resonance frequency.

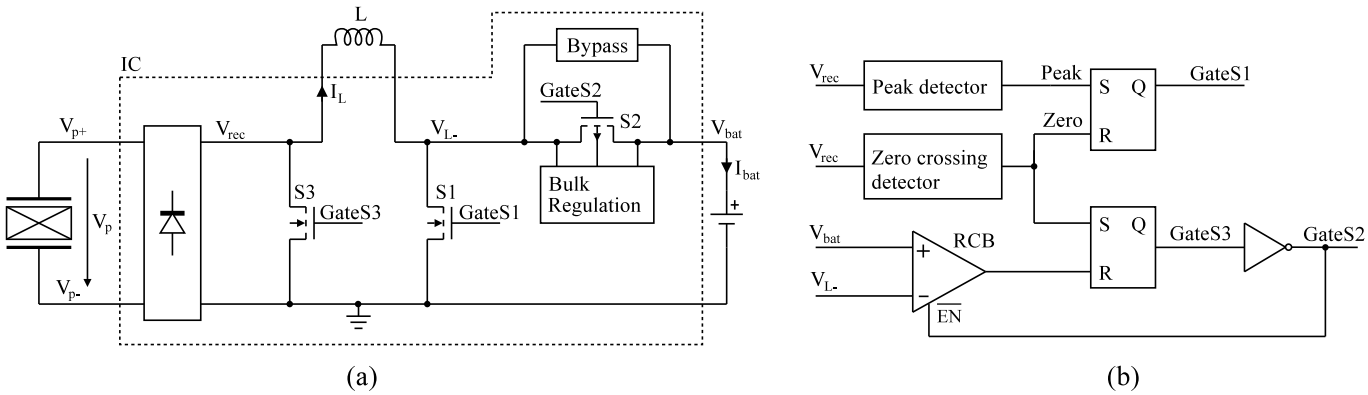

Fig. 2: Block diagram showing (a) the interface circuit and (b) the controlling unit generating the switch MOSFET control signals.

the PZT. Thus, the PZT voltage is not clamped and is therefore able to rise to its maximum. The duration of phase A is in the range of the source frequency, i.e. some milliseconds.

When the maximum of V_{rec} is detected, the transfer process consisting of phases B and C begins. During phase B, switch S1 closes, forming an oscillating circuit between the piezo capacitor and the inductor. While energy is being transferred from the piezo capacitor into the inductor, I_L is rising, whereas V_{rec} is falling. Phase B terminates when V_{rec} has reached 0V.

Once V_{rec} has reached 0V (which corresponds to a maximum of I_L), phase C is initiated, which means that S1 opens and S2 and S3 close. Hence, the inductor delivers its energy into the battery, causing I_L to fall. When I_L reaches 0A, i.e. at the end of phase C, the transfer process stops, S2 opens, and the procedure restarts with phase A. It is extremely important that S2 is opened before I_L gets negative in order to avoid current back flow. The oscillating circuit given by C_p and L defines the length of phases B and C, which are together in the microsecond range. Thus, the transfer process is much shorter than phase A. Note that V_{rec} is always positive due to the rectifier.

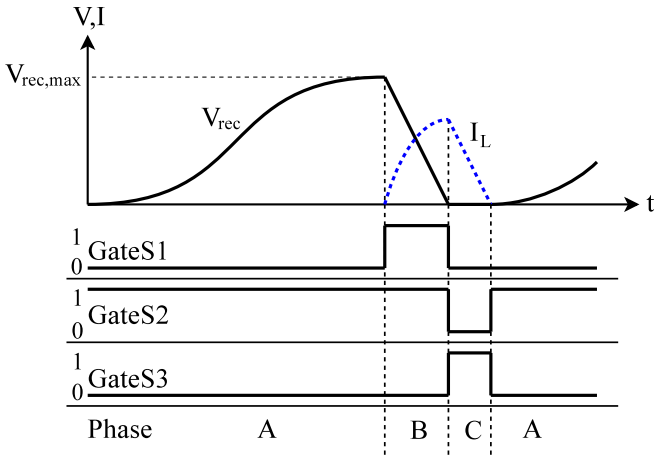

Fig. 3: Timing diagram of the control signals for the MOSFET switches.

3. CIRCUIT IMPLEMENTATION

The dashed box in Fig. 2(a) marks the interface circuit which is implemented in a 0.35 µm CMOS process. Transistors which are directly connected to the PZT are 5 V-MOSFETs with thick oxide. With these transistors, the maximum applicable PZT voltage is 7 V. Otherwise, standard 3.3 V-MOSFETs are used. A drawback of the 5 V-transistors is the high threshold voltage of around 1.2 V. Due to this the W/L ratio has to be increased in order to maintain low *on*-resistance. The only components which have to be connected externally are the PZT, the inductor and the battery.

The interface circuit mainly consists of the rectifier, the switches S1, S2, S3 and the controller for the switches which is shown in Fig. 2(b). The controller is supplied by the battery, implying that the power consumption of the controller has to be very low, i.e. in the microwatt range. This is achieved by (i) dynamically switching *on* and *off* the control blocks and (ii) biasing the analog circuitry with a very low current of about 20 nA. The battery is charged passively by the PZT via a bypass if V_{bat} is below a threshold of about 1.2 V which corresponds to the threshold voltage of the 5 V-transistors.

The rectifier is taken from [3]. It consists of a an active and a passive CMOS rectifier connected in parallel. The active rectifier works only if V_{bat} is large enough, providing highly efficient rectification. If V_{bat} is below the minimum operating voltage, rectification is nevertheless guaranteed by the passive rectifier. The dimensions of the rectifier transistors are given in Table 1.

The switches S1, S2 and S3 are also realized as MOSFETs. Since the conversion efficiency strongly depends on the ohmic resistance in the signal path of I_L, it is crucial to reduce the *on*-resistance of these transistors. The corresponding W/L ratios are listed in Table 1. The introduction of switch S3 is an improvement with regard to the circuit in [3], because there the current path is closed via the body diodes of

Table 1: Electrical specifications.

Circuit	
V_{bat}	2 V
L	100 µH
R_L	1 Ω
$(W/L)_{switchFETs}$	20 mm/1 µm
$(W/L)_{rectifierFETs}$	20 mm/1 µm
Generator	
$(\omega/2\pi)_{resonance}$	250 Hz
I_p	80 µA ... 230 µA
V_p	2.4 V ... 7 V
C_p	12 nF
R_p @ 250 Hz	36 kΩ
Peak detector	
I_{ref}	20 nA
C_s	50 pF

the rectifier MOSFETs, leading to a non-negligible power loss and hence to an overall efficiency reduction.

Fig. 4 shows the peak detector which generates a short pulse when V_{rec} starts falling after having crossed a voltage maximum. This event initiates phase B (S1 conducts). One goal in the circuit development was to allow PZT voltages that are higher than V_{bat}. Due to this, it is not possible to use conventional peak detectors based on voltage comparators like the version presented in [3]. One solution to overcome this problem is to convert the voltage V_{rec} into a current I_s through a series capacitor C_s and to compare I_s with a small fixed current I_{ref}. As long as V_{rec} is rising fast, C_s is being charged with a large current. When V_{rec} is approaching a maximum, I_s is getting smaller until it falls below I_{ref}. This event causes the current comparator to generate a pulse indicating that a peak has occured. After this pulse, C_s is discharged to make the peak detector ready for a new cycle. C_s has to be dimensioned carefully. On the one hand, it is advisable to choose a small capacitance in order to reduce the power loss caused by the current flow. On the other hand, I_{ref} should not be in the region of leakage since this could affect the moment of switching. Appropriate values can be found in Table 1.

The zero crossing detector is taken from [3]. This block generates a short pulse when a threshold of about 0.3 V is crossed, causing S1 to stop conducting and at the same time S2 and S3 to close. This event indicates that the energy from the piezo capacitor has been transferred completely to the inductor.

Another crucial component of the interface circuit is the reverse current blocking (RCB) based on the active diode concept presented in [7]. The RCB mainly consists of a fast comparator that raises its output when V_{L-} is lower than V_{bat} indicating a reverse current that would discharge the battery. Since the RCB

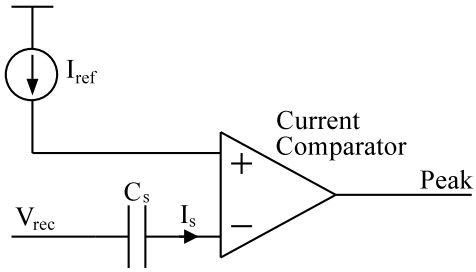

Fig. 4: Capacitively coupled high voltage peak detector.

comparator consumes much power, it is activated by the zero crossing detector and deactivated immediately after reverse current detection. Thus, it is enabled only for some microseconds, keeping the average power consumption low.

4. RESULTS

The circuit has been simulated using Cadence Spectre in a 0.35 µm technology. A 2 V DC voltage source models a fully charged battery.

The waveforms of the rectified voltage V_{rec} for different PZT current amplitudes are shown in Fig. 5. The smaller peaks exist because of the relatively low PZT internal resistance R_p. Fig. 5 shows that the circuit operates properly over the given range. This distinguishes the proposed circuit from the circuit presented in [3] whose timing is only correct for a fixed $V_{rec,max}/V_{bat}$-ratio.

Proper operation has been evaluated for PZT amplitudes from 2.4 V to 7 V. The timing of the circuit is adjusted to work fine with the resonance frequency of the commercial PZT bending generator [5] that is given as 250 Hz. Frequency sweeps from 50 Hz to 1000 Hz suggest that the circuit also works in this frequency range.

In order to obtain a high conversion efficiency, it is essential to reduce the power consumption of the controller as much as possible. In the current design, a very low average power consumption of about 1.3 µW has been achieved by dynamically switching *on* and

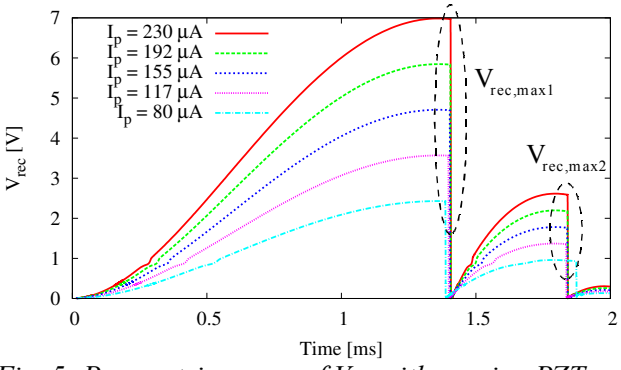

Fig. 5: Parametric sweep of V_{rec} with varying PZT current amplitudes, plotted over a half period.

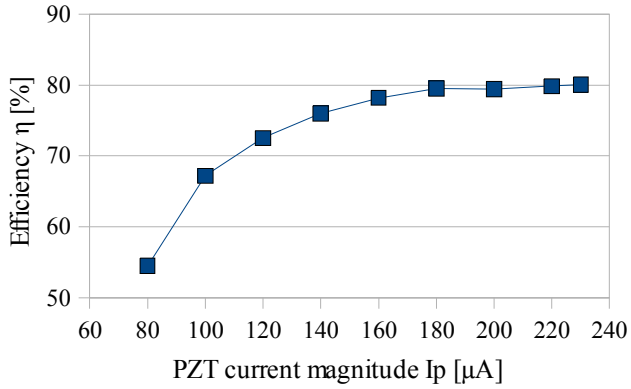

Fig. 6: Simulated efficiencies for different excitation amplitudes.

off the separate control blocks.

The average output power is determined according to equation (1) by integrating the current flow into the battery I_{bat} over a half period; V_{bat} is assumed to be constant.

$$\overline{P_{out}} = \frac{1}{T/2} V_{bat} \int_0^{T/2} I_{bat}\, dt \tag{1}$$

The energy stored in the piezo capacitor at the beginning of the transfer process divided by the cycle time represents the average input power, as can be seen in equation (2). $V_{rec,max1}$ and $V_{rec,max2}$ are the piezo capacitor voltages at the beginning of the first and the second transfer process (see Fig. 5).

$$\overline{P_{in}} = \frac{1}{T/2} \int_0^{T/2} P_{in}\, dt = \frac{1}{T/2} 0.5\, C_p \left(V_{rec,max1}^2 + V_{rec,max2}^2 \right) \tag{2}$$

The efficiency of the converter η is defined as the ratio of the average output power to the average input power:

$$\eta = \frac{\overline{P_{out}}}{\overline{P_{in}}} = \frac{V_{bat} \int_0^{T/2} I_{bat}\, dt}{0.5\, C_p \left(V_{rec,max1}^2 + V_{rec,max2}^2 \right)} \tag{3}$$

Fig. 6 shows that the efficiency starts with 53% for a low PZT current amplitude of 80 µA (which corresponds to a PZT amplitude of 2.4 V) and rises quickly to values above 80% as I_p increases. This behavior is due to the fact that the absolute power consumption of the control circuit is constant and dominates when the PZT voltage is low. Presumably the efficiency will decrease when I_p rises further due to a higher voltage drop over the switches.

5. CONCLUSION

A self-clocked CMOS integrated interface circuit for piezoelectric generators (PZT) has been presented. Proper operation has been evaluated for PZT amplitudes from 2.4 V to 7 V and excitation frequencies from 50 Hz to 1000 Hz with a supply voltage of 2 V (operable down to 1.2 V). By keeping the power consumption of the controller as low as 1.3 µW, simulation suggests that conversion efficiencies of 80% can be achieved. The upper limit of the allowed PZT voltage amplitude can be increased using high voltage transistors, but this will result in higher threshold voltages thus leading to higher power consumption and lower efficiency.

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