BASIC CHARACTERISTICS OF DIGITALLY CONTROLLED BOOST TYPE DC-DC CONVERTER

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Abstract: This paper presents the basic characteristics of the digitally controlled boost type dc-dc converter. The static and dynamic characteristics of the dc-dc converter with the digital PID control are discussed. Especially, it is examined that the A-D conversion timing and anti-aliasing filter's cut-off frequency affect the dynamic and static characteristics. As a result, when the anti-aliasing filter's cut-off frequency is low, the range of unevenness of output voltage by the difference of A-D conversion timing is small. However, in the dynamic characteristics, the transient time is long and there is no difference against the A-D conversion timing.

Key words: Digital control**,** Boost type dc-dc converter, A-D conversion timing, anti-aliasing filter, cut-off frequency

1. INTRODUCTION

Recently, the concern with energy management in clean energy system has been growing. In this case, the boost converter is usually used in order to receive from the clean energy source, that is, solar cell, fuel cell and so forth because the input current of boost converter flows always continuously[1]-[4].

On the other hand, the high controllability and monitoring function are required in these systems. So, the digitally controlled switching power supply is useful because it has the advantage of realizing both control and monitoring tasks. Furthermore, a key distinguishing feature of digital control circuit is easily able to communicate to the other component in the electronics system.

However, there has been no study that tried to discuss the digitally controlled boost type dc-dc converter in detail.

This paper presents the basic characteristics of the digitally controlled boost type dc-dc converter. The input reactor current of the boost converter is continuous. But, the output diode current is discontinuous. Therefore, the ripple of the output voltage is relatively large. So, the relationship between the sampling point during a switching period and the regulation characteristics is clarified. In this paper, the static and dynamic characteristics of the dc-dc converter with the digital PID control are discussed. Especially, it is examined that the A-D conversion timing and anti-aliasing filter's cut-off frequency affect the dynamic and static characteristics.

2. CIRCUIT CONFIGURATION AND OPERATION PRINCIPLE

Figure1 shows the block diagram of the proposed digitally controlled boost type dc-dc converter using DSP. E_i is the input voltage, and e_o is the output voltage. T_r is the main switch, D is the fly wheel diode, L is the energy storage reactor, C is the output smoothing capacitor and R is the loa-d. The output voltage e_o is sent to the A-D converter through the anti-aliasing filter and is converted into digital amount N_n. The relation between the input and output values of the a-d converter is given by equation (1) when it approximately shows the linear expression by considering the width of the quantization to be small. where n denotes an n-th switching cycle, and the digital amount N_n is a positive integer number. $G_{A\text{-}D}$ is a gain of the A-D converter and given by equation (2).

$$N_n = G_{AD} e_n \tag{1}$$

$$G_{A-D} = \frac{N_{n,max}}{e_{o,ADmax}} \tag{2}$$

The digital amount N_n is sent to DSP. In DSP, the numerical value N_{Ton} that corresponds to the on-time interval T_{on} is calculated.

The relation between the on-time interval T_{on} and the numerical value N_{Ton} is shown as follows;

$$\frac{T_{on,n+1}}{T_s} = \frac{N_{Ton,n+1}}{N_{Ts}} \tag{3}$$

where N_{Ts} is a numerical value corresponding to the switching period T_s (=1/f_s). N_{Ts} is calculated in the PWM signal generation circuit which is composed of a-digital comparator or a counter. This case the PWM signal generation circuit is composed of a counter. Counter's frequency is f_{ck}, and relation between N_{Ts} and f_{ck} is given by equation (4).

$$N_{Ts} = f_{CK} T_s \tag{4}$$

The relation between $T_{on,n+1}$ and $N_{Ton,n+1}$ is shown as follow by using equation (4);

$$\frac{T_{on,n+1}}{T_s} = \frac{N_{Ton,n+1}}{f_{CK} T_s} \tag{5}$$

According to the relation between the on-time interval T_{on} and the numerical value N_{Ton}, T_{on} is generated. This T_{on} regulates the output voltage e_o.

The on-time interval N_{Ton} of the P-I-D control circuit is represented as follows [5], [6];

$$N_{Ton,n+1} = N_B - K_P(N_n - N_R) - K_I \sum (N_n - N_{INT}) - K_D(N_n - N_{n-1}) \tag{6}$$

where K_P, K_D and K_I are the proportional, differential and integral coefficients. N_B is the numerical bias value. N_R and N_{INT} are the numerical proportional and integral desired values, these values are shown as follows;

$$N_B = N_{TS}\left(1 - \frac{E_i}{E_o^*}\right) \tag{7}$$

$$N_{INT} = G_{AD} e_o^* \tag{8}$$

The switching noise is generated when the switch is turn off or turn on. To guard the switching noise of output voltage ripple, the A-D conversion timing of output voltage is very important for digital controlled dc-dc converter shown Fig. 1. Figure 2 shows the observed input waveforms of the A-D converter. Figure 2(a) shows the waveform when the anti-aliasing filter's cut-off frequency is 25 kHz. Figure 2(b) shows when anti-aliasing filter's cut-off frequency is 50 kHz. In these figure, the upper waveform is the input signal of the A-D converter and the under waveform is the signal S_{Ton}. As shown in these figures, when anti-aliasing filter's cut-off frequency is low, the peak values of the switching noise and ripple of the output voltages are low.

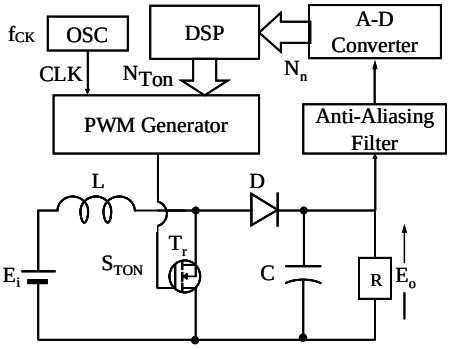
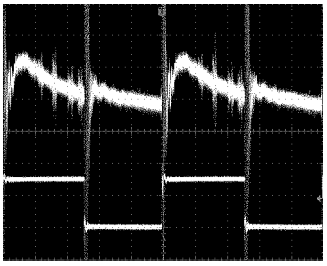
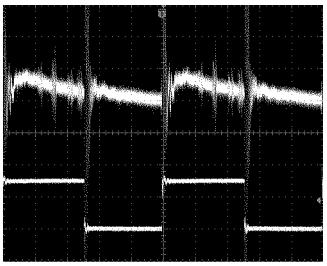


Fig. 1 Block diagram of digitally controlled boost type dc-dc converter using DSP.



Vertical 100mV/div.
Horizontal: 2μs/div.
(a) fc=50kHz.



Vertical 100mV/div.
Horizontal: 2μs/div.
(b) fc=25 kHz.

Fig. 2 Observed Input waveforms of A-D converter.

3. EXPERIMENTAL RESULTS

Figure 3 shows the A-D conversion timing to discuss the effect of the influence of the output voltage ripple and switching noise. The switching frequency is 100 kHz and the sampling frequency is also same. So T_s is 10μs. When the switch is turn on, the time of the A-D conversion timing is 0. The four sampling points

are t_{s1}=2.5μs, t_{s2}=4.5μs, t_{s3}=7.5μs and t_{s4}=9.5μs as shown in this figure. And the input voltage E_i is 10V, the desired voltage E_o^* is 20V, the inductance L is 500μH, the output capacitance C is 470μF, and the number of bit of the A-D converter is 8bits.

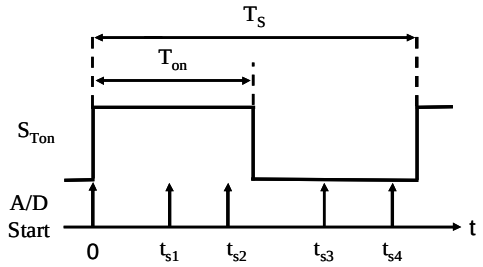


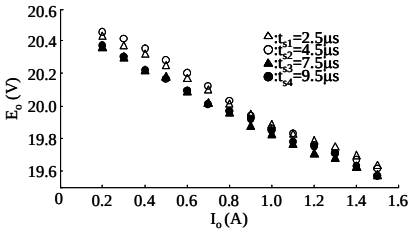
Fig. 3 A-D conversion timing.

3.1 Static Characteristics

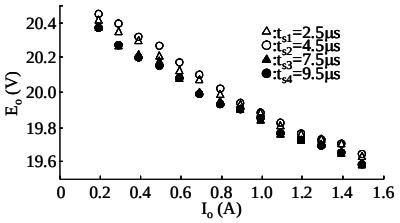
Figure 4 shows the regulation characteristics in case of K_P=1. Figure 4(a) shows the regulation characteristics when the anti-aliasing filter's cut-off frequency is 50 kHz, and Fig. 4(b) shows when it is 25 kHz. Then the range of the unevenness of output voltage by the difference of A-D conversion timing is 140mV in 50 kHz and 130mV in 25 kHz, respectively.

Figure 5 shows the regulation characteristics in case of K_P=3. Figure 5(a) shows when the anti-aliasing filter's cut-off frequency is 50 kHz, Fig. 5(b) shows when it is 25 kHz. The range of unevenness of output voltage is 310mV in 50 kHz and 170mV in 25 kHz.

From these figures, it is seen that the range of unevenness of output voltage by the difference of A-D converter's timing becomes larger when KP is larger. However, when the anti-aliasing filter's cut-off frequency is lower, the range of unevenness of output voltage by the difference of A-D converter's timing is lower.

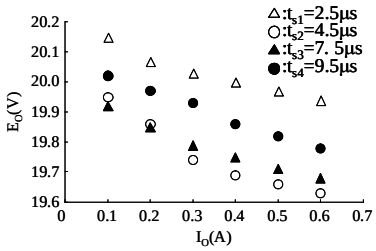


(a) fc=50kHz.

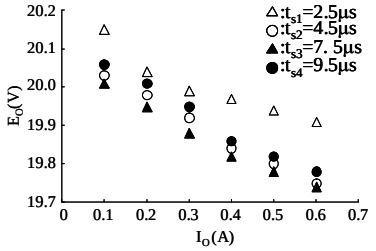


(b) fc=25kHz.

Fig. 4 Regulation characteristics in case of K_P=1.



(a) fc=50 kHz.



(b) fc=25kHz.

Fig. 5 Regulation characteristics in case of K_P=3.

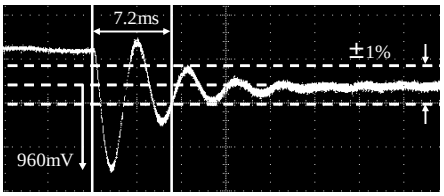
3.2 Dynamic Characteristics

Figure 6 shows the observed waveform of the experimental dynamic characteristics in the P control. In this figure, the step change of the loa-d R is from 100Ω to 20Ω and the A-D conversion timing is t_{s4} (=9.5μs). Figure 6(a) shows the waveform when the anti-aliasing filter's cut-off frequency is 50 kHz and Figure 6(b) shows that the anti-aliasing filter's cutoff

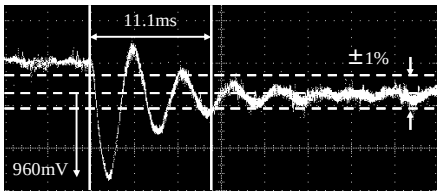
frequency is 25 kHz, respectively. When the anti-aliasing filter's cut-off frequency is 50 kHz, the transient time is 7.2ms and undershoot is 960mV.When the anti-aliasing filter's cut-off frequency is 25 kHz, the transient time is 11.2ms and the undershoot is 960mV. From these figure, when anti-aliasing filter's cut-off frequency is higher, the transient time is longer. Moreover, by changing A-D conversion timing, the transient time and undershoot are no difference.

Figure 7 shows the observed waveform of the experimental dynamic characteristics in the PID control. The other circuit and measured condition are same to Fig. 6. The proportional coefficient K_P, the differential coefficient K_D and the integral coefficient K_I are 0.3, 1.0 and 0.001, respectively. Figure 7(a) shows the waveform when the anti-aliasing filter's cut-off frequency is 50 kHz and Fig. 7(b) shows when the anti-aliasing filter's cut-off frequency is 25 kHz. When the anti-aliasing filter's cut-off frequency is 25 kHz, the transient time is 14.2ms and the undershoot is 1.61V. When the anti-aliasing filter's cut-off frequency is 50 kHz, the transient time is 14.2ms and the undershoot is 1.61V. The digital controlled boost

type dc-dc converter with the PID control has no different characteristics against the change of the A-D conversion timing and anti-aliasing filter's cut-off frequency because these cut-off frequencies are relatively high.

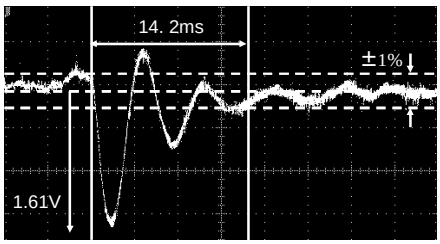


Vertical 500mV/div.
Horizontal: 4ms/div.
(a) fc=50 kHz.

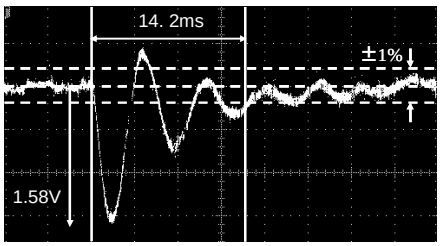


Vertical 500mV/div.
Horizontal: 4ms/div.
(b) fc=25 kHz.

Fig. 6 Indicial response of digital P control.



Vertical 500mV/div.
Horizontal: 4ms/div.
(a) fc=50 kHz.



Vertical 500mV
Horizontal: 4ms/div
(a) fc=50 kHz

Fig. 7 Indicial response of digital P-I-D control.

4. CONCLUSIONS

In the digital controlled boost type dc-dc converter in the P control and the PID control using the DSP, it is discussed that the A-D conversion timing and anti-aliasing filter's cut-off frequency affect the dynamic and static characteristics.

From the above discussion, when anti-aliasing filter's cut-off frequency is low, the range of unevenness of output voltage by the difference of A-D converter's timing is lower in the regulation characteristics. In the dynamic characteristics, when anti-aliasing filter's cut-off frequency is low, the transient time is long. On the other hand, the digital controlled boost type dc-dc converter has no different characteristics by changing the A-D conversion timing.

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