ELECTROSTATIC NANO-SUPERCAPACITORS FOR ENERGY STORAGE

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Abstract: The fabrication of 3-d nanostructures can serve as building blocks for a vast range of on-chip energy storage devices. The ability to precisely control material deposition inside these structures is attractive due to its potential for integration with conventional fabrication technology commonly used in MEMS and NEMS devices. This talk discusses how two key-processing technologies, namely anodic aluminum oxide (AAO) and atomic layer deposition (ALD) are implemented to create metal-insulator-metal (MIM) nanocapacitors. These highly scalable processes produce structure arrays exhibiting high power and energy densities, which makes such structures ideal for integration systems-on-a-chip technology where autonomous energy generation and storage is required.

Keywords: MIM nanocapacitor arrays, Anodic Aluminum Oxide (AAO), Atomic Layer Deposition (ALD)

INTRODUCTION

The strategy for making nano supercapacitor arrays with ALD and AAO by enhancing surface-to-volume ratios, provide an opportunity to create novel devices with enhanced energy storage properties whilst maintaining the high power density characteristic of electrostatic capacitors. The combination of self-assembly, ordering, uniformity and conformality on a nanoscale are extremely advantageous for integration with MEMS and NEMS based devices which require on-chip power to drive circuits, sensors and mechanical components.

The MIM nanocapacitors built inside AAO templates using an all ALD processing sequence demonstrates a powerful combination of highly scalable processes yielding energy storage devices.

The combination of self-ordered, densely packed ($10^{10}cm^{-2}$) nanopores of AAO[1] and the multi-layer, self-limiting and conformal coating of complex 3D surfaces by ALD[2] enables us to create massively parallel supercapacitor arrays consisting of more than a million nanocapacitors in every device. As shown in a Ragone Plot in Figure 1, our devices exhibit high power density of traditional electrostatic capacitors while matching the energy densities of conventional electrochemical capacitors thus ushering in a new era of energy storage devices.

Unlike other thin film deposition techniques, ALD allows monolayer control of film thickness and provides uniformity within AAO template. In addition, ALD is a self-limiting chemisorption process that allows uniform deposition of material over the entire surface area, even over complex 3D structures like AAO.

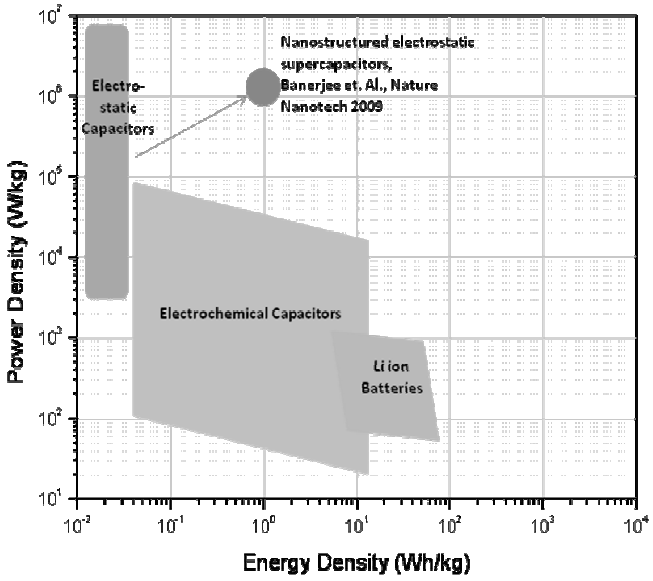

Figure 1: Ragone Plot shows MIM high energy density and high power density.

In this paper, we show MIM nanocapacitors comprising of Al-doped ZnO electrodes sandwiching an insulator layer consisting of a bilayer TiO2-Al2O3 inside AAO pores up to 1μm deep. Capacitance data indicate the nanocapacitors are being engineered to specification. We discuss challenges overcome while processing these nanocapacitors and elucidate current strategies to make these devices more reliable.

MIM DEVICE FABRICATION

High purity, 250µm Al films (Alfa Aesar) are electropolished in a 5:1 perchloric and ethanol solution. The AAO pores are then formed by a two-step anodization process as described by Masuda et al[1] [1]. Anodization of these Al films in oxalic acid results in a hexagonally ordered porous membrane with a number density of ~$1.1x10^{10}cm^{-2}$, pore diameters of ~35nm and interpore spacings of ~110nm.

Pore depths can easily be controlled because they are dependent on anodization time at the rate of 72nm/min. MIM capacitors have been built on first anodized Al (scalloped surface texture) and second anodized porous AAO templates ranging from 500nm to 10µm in pore depth. First anodized Al surface is obtained after the AAO formed

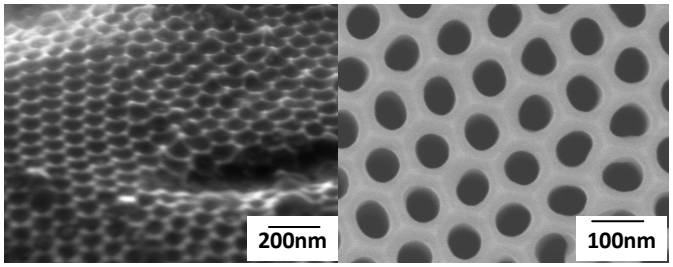

Figure 2. SEM images of first anodized Al surface (left) and top-view of pore-widened AAO (right).

during initial anodization is stripped, leaving the bare and scalloped Al surface. Porous AAO templates are obtained from a second anodization on first anodized Al surfaces. SEMs these Al/AAO structures are shown in Figure 2. Pore diameters can also controlled by etching the second anodized porous nanostructure in a 1:1 NH_4OH and Deionized H_2O solution. The pore widening rates are also time dependent and can be increased to ~80nm.

After AAO template fabrication, ALD is utilized to create the MIM structure within the highly ordered, porous AAO material because of its ability to conformally coat inside high aspect ratio (AR) nanostructures. A layer of metal, insulator and metal thin films are deposited. The metal layer consists of TiN[3] or conducting Al-doped ZnO (AZO) ~7-10nm thick and the insulating layer consists of Al_2O_3 (~6-7nm thick). Conventional photo and masking steps are then used to create the top electrodes for electrical testing.

Past work has shown workable TiN/Au electrodes but recent work has focused on the MIM structure made with AZO-TiO_2-Al_2O_3-AZO layers. Here, photolithography of the AZO top electrode (deposited via ALD) can easily be achieved; therefore this offers a cheaper and simple alternative when compared to patterning and etching process for Au or Al metal contacts. Notice than an additional titania layer has been incorporated in the insulating layer as an etch-stop layer, preventing etching of insulator or the bottom electrode (BE) when patterning the top electrodes.

Device characterization is performed with a fully automated home built probe station connected to an LCR meter (Agilent E4980), HP Semiconductor Parameter Analyzers 4140B and 4155C. We were able to obtain quasi-static CV measurements and IV curves of the capacitors. SEM analysis has also been performed on a Hitachi SU-700 analytical SEM.

RESULTS

SEM cross-section of MIM capacitor in 500nm and AAO template is shown in Figure 3. Images show ALD conformally coats the high aspect ratios of the AAO template thus forming the MIM structure inside every pore.

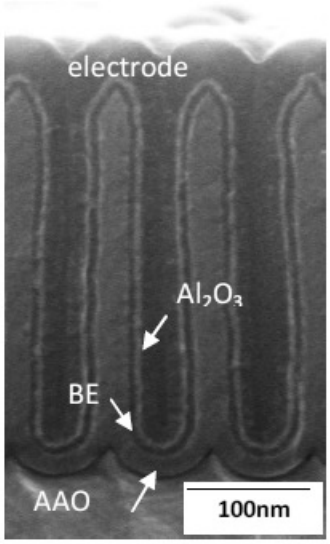

Figure 3. SEM cross section of 500nm MIM capacitors in AAO templates.

CV and IV measurements were taken for planar MOS capacitors, first anodized Al surfaces and 500nm, 1µm and 2µm AAO pore depths all with the same patterned 0.250mm diameter electrodes. The capacitance results were normalized with respect to the planar footprint area of each capacitor. This is termed as Equivalent Planar Capacitance (EPC)[4].

The MOS capacitance is given by the equation for planar capacitance,

$$C = \frac{k\varepsilon_o A}{d} \quad (1)$$

With an understanding of the geometrical parameters, the EPC for porous AAO templates can be modeled by the following equation:

$$C_{total} \sim \alpha\,(C_{planar} + C_{pore} + C_{bottom}) \quad (2)$$

Where,

$$C_{planar} = \frac{k\varepsilon_o}{t_{insulator}}\left(\frac{\sqrt{3}}{2}\left(2r_{pore} + D\right)^2 - \pi r_{pore}^2\right) \quad (2a)$$

$$C_{pore} = \frac{2\pi k\varepsilon_o L}{\ln\left(\frac{r_{pore} - t_{BE}}{r_{pore} - \left(t_{BE} + t_{insulator}\right)}\right)} \quad (2b)$$

$$C_{bottom} = k\varepsilon_o \frac{\pi\left(r_{pore} - (t_{BE} + t_{insulator})\right)^2}{t_{insulator}} \quad (2c)$$

Figure 4 shows a graph of capacitance values as a function of pore depth. Fabrication of MIM structures in AAO templates has a dramatic capacitance enhancement over MOS Caps, which only show a EPC of ~1µF/cm^2, as can easily be seen in the figure. The linear fit data is given by the EPC model. Capacitance values scale with the depth of the pores – planar, 500nm and 1µm measure 1µF/cm^2, 9.4µF/cm^2, 13.6µF/cm^2, respectively. These values are in line with the predicted values determined by the equations above. The capacitors were also tested for their reliability by ramping voltage till breakdown. Figure 5 shows the Weibull plot of the breakdown field for Si/SiO_2 planar, first anodized, 500nm, and 2µm AAO templates. The MOS capacitor shows the highest breakdown field of 12MV/cm. The breakdown field is much lower for first anodized, 500nm and 2µm AAO MIM capacitors and lies between 10^{-1} and 3MV/cm fields. It is interesting to note that the breakdown fields for Al surface and AAO MIM capacitors are very similar.

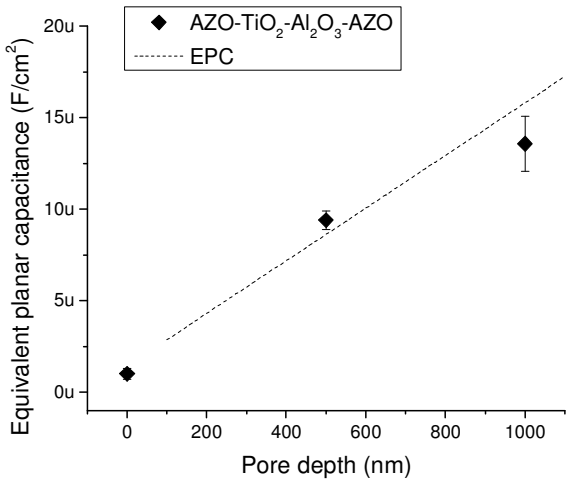

Figure 4. EPC for on planar Si/SiO_2, 500nm, 1µm calculated with insulator dielectric constant of 7.3.

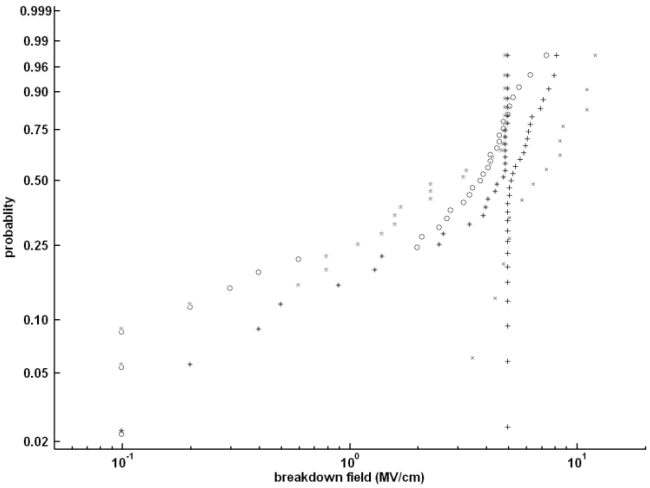

Figure 5. Weibull of probability breakdown field for MIM built on planar Si/SiO_2 (+), first anodized Al (○), 500nm (□) and 2µm (◇) structures.

DISCUSSION

The reliability behavior of the Al surface and AAO based MIM capacitors can be related to specific structural features that are thought to significantly influence breakdown fields and leakage currents of these devices. Specifically, premature breakdown in dielectrics is attributed to surface asperities and roughness of AAO templates. It is well known that AAO pores are separated by sharp peaks created as a result of the unique nature of self ordering that occurs via the establishment of dynamic equilibrium between alumina etching and growth processes during AAO pore formation. These peaks act as areas of high, local electric fields, thus becoming the dominant defects causing dielectric breakdown. Furthermore, these peaks tend to increase in size at domain boundaries. Figure 6a shows an SEM top-view of a full first anodized Al surface. Domains boundaries are observed at bright spots in SEM photo. When depositing MIM layers onto the AAO, these peaks create high local electric fields at the electrode - insulator interface which induce premature breakdown and high leakage. The sharp asperities are a common feature of the Al stripped surfaces and the AAO templates irrespective of the pore depths. This explains why the Al stripped surface and AAO based MIM capacitors show similar breakdown fields.

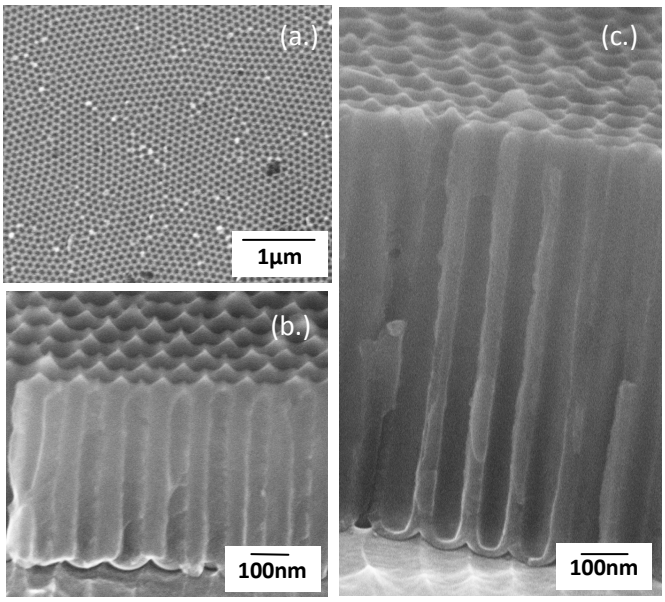

Figure 6. a) first anodized Al surface b)500nm pores without RIE etch shows sharp peaks and c) 1µm pore with RIE etch shows rounded peaks.

Increasing thickness of BE rounds the peaks off and may aid in increasing breakdown field. However, it is required that the MIM layers be of optimal thickness for high capacitance and low leakage, thus making this pathway unattractive. Instead, Reactive Ion Etching (RIE) can be implemented after second anodization to round the sharp asperities between pores. Initial research has proven this as a valid option.

Figure 6b and 6c shows how this isotropic aluminum/alumina etching rounds the peaks. In addition, the RIE etching also drastically reduces the size of larger defects found along domain boundaries. Another source of defects influencing electrical characteristics can be from impurities introduced by the oxalic acid during anodization. Pore widening removes most crystallites. However, AAO membrane contains a denser inner layer and a more porous outer layer[5]. Mobile ions can be trapped in this layer, directly influencing the electrical reliability of films deposited in AAO structure. To avoid effects of mobile ions, more alumina from AAO structure can be etched away and fresh Al_2O_3 layers can be deposited (via ALD) into the pores, acting as a diffusion barrier for mobile ions. Initial work has proven an I-MIM structure does improve electrical breakdown/leakage with the addition of such a bottom "inactive" layer. Further work will implement all these strategies together to realize the collective advantage of the processing steps in making MIM based nano supercapacitors reliably viable as an on-chip high power source.

CONCLUSION

In this paper we have discussed the processing and characterization techniques of MIM nanocapacitors using an ALD sequence and AAO templates. By implementing such techniques, MIM capacitors can be built with great control at nano-scales. Our MIM this far has shown a dramatic improvement in the equivalent planar capacitance as compared to current recorded information.

Overall, the MIM nanocapacitors built inside AAO templates using an all ALD process sequence demonstrates a powerful combination of highly scalable processes to yield attractive energy storage devices. We have demonstrated that this combination leads to a self-aligned nanostructure that is uniform in its structure and properties across large arrays comprising of more than one million nanocapacitors. Strategies such as those described in this paper are key enabling features for integration of such devices with system-on-a-chip which require autonomous energy generation and storage. Further optimization of the device structure will provide a well-suited device for such integration.

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