CMOS-INTEGRATED ADAPTIVE LOAD MATCHING INTERFACE WITH AN INTEGRATED LOAD MATCHING DETECTOR

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Abstract: This paper reports on a manufactured fully-integrated impedance matching interface for energy harvesting transducers together with a novel load matching detector. As measurements show, the main achievements are (1) adaptive input load matching, that means the excited transducer is almost ideally loaded, and (2) the implicit voltage up-conversion, which allows generator output current flow even when the buffer voltage is higher than the actual open circuit generator voltage $V_{gen,0}$. In addition, (3) a novel integrated low-power method is introduced for sensing the actual open-circuit voltage and detecting load matching condition even while the excited generator is loaded.

Keywords: generator interface circuit, voltage conversion, impedance matching (detector)

INTRODUCTION

The number of reasonable autonomous operating applications and small electronic systems rises, because there is a significant gain by using these divers ambient powering sources, concluded as micro energy harvesting (µEH) systems [1].

Among those energy transducers, vibration driven transducers are very frequently presented. In terms of energy transduction or source efficiency, basically all of them suffer from large internal source impedances. That means, most power output is only achievable in conjunction with sufficient impedance matching. Thus, a certain transducer interfacing circuit is required [2]. In the field of piezoelectric transducers there are competing techniques of continuous impedance matching and pulsed amplitude synchronized techniques are presented. The efficient technique of synchronous charge extraction was successfully established. Such interfaces allow lager mechanical amplitudes due to reduced electrical damping. This results in multiples of output power compared to classical continuous impedance matching [2].

In the field of electro-dynamic or inductive transducers exist only few work about such interface circuits. Reasons might be the typical low voltage levels, which are difficult to handle in terms of circuit design, and second, due to the current and coil based different physical and technical nature, such pulsed techniques seem not applicable or at least have not been presented and discussed so far, to the best of our knowledge. Thus, only continuous load matching techniques seem feasible.

The difficulty of continuous load matching is that the actual load is a storage device, which should not dissipate any energy. Therefore, an intermediate interface stage is necessary (Fig. 1). This stage has to apply appropriate equivalent load impedance to the generator for impedance matching achievement. Simultaneously, the generator power has to be efficiently transferred into an energy storage device. That requires voltage conversion as well as continuous control of the matching conditions. While voltage conversion is not a major problem – there are plenty of methods and systems – retaining the matching condition is challenging, since the actual generator power, voltage or current is not known due to mostly random external excitation.

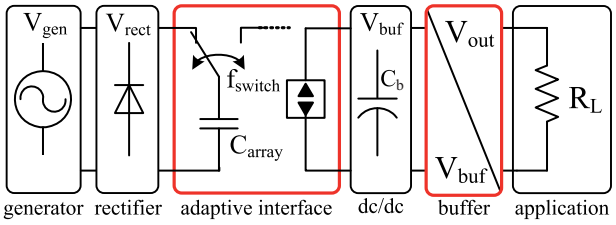

Fig. 1: An adaptive interface is required between rectification and storage.

This paper presents a fully-integrated 0.35 µm CMOS chip for obtaining adaptive impedance matching and efficient energy storage, while driven by an electro-dynamic transducer. Furthermore, a novel technique and circuit for the necessary detection of load matching condition was developed and is presented.

The impedance matching principle, chip implementation and operation of the adaptive interface is given in Section II. Next, the method and basic circuit design of the load matching detector (LMD) is presented in Section III. Further on, measurements of the interface chip are discussed in Section IV. Finally, Section V concludes the paper.

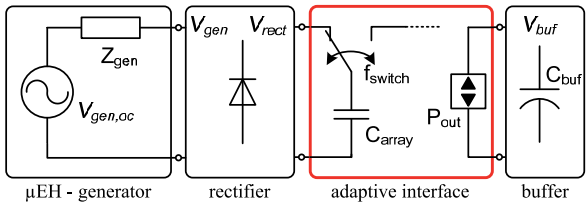

Fig. 2: Load matching interface presents a charge controlled and toggling capacitance to the generator.

LOAD MATCHING INTERFACE

As presented in [3], a power source with source resistance R_{gen} provides the most power during charging a capacitor C_{in} only in the region around $\ln(2) \times R_{gen} C_{in}$. Thereby, the actual capacitor voltage coincides with the half of the actual open circuit voltage of the source, which equals the impedance matching conduction.

In order to evaluate this principle an interface systems was implemented, which is particularly intended for electro-dynamic transducers (Figures 2 and 3). This generator interfacing converter comprises two oppositional toggling capacitor arrays. At a time, one array is connected to the rectifier (Fig. 4) and the other array is connected to the buffer. This way, there is always a capacitor array, which is being charged by the transducer, while the other array is discharging its energy into the buffer. Using arrays with three capacitors each is done for voltage conversion reasons. The actually charged array has all capacitors connected in parallel, while for discharging the capacitors are stacked so as to exceed the buffer voltage.

The transient operation is clarified with the measured plots in Figures 5. The subsequent charging and discharging waveforms are only shown for one capacitor array.

For adaptive control of the charging, discharging and voltage conversion due to capacitor stacking, the interface systems includes a charge control unit (CCU) as well as a ratio control unit (RCU), as illustrated in Figure 6.

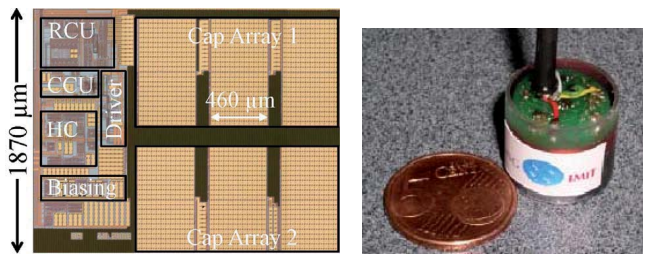

Fig. 3: Micro photography of the interface chip (a) and the inductive generator (b).

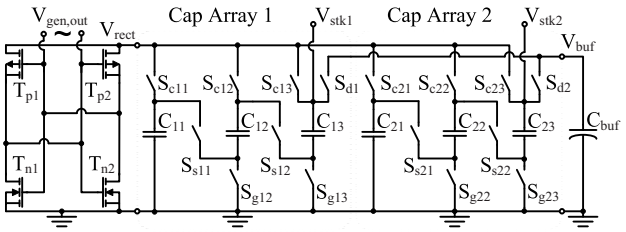

Fig. 4: Switched capacitors of the interface are located between the rectifier and the buffer.

The load matching detector (LMD) provides a trigger signal V_{match} to the CCU to signalize that efficient charging and load matching region is left. Based on this signal, the CCU can initiate that both arrays toggle to the opposite state.

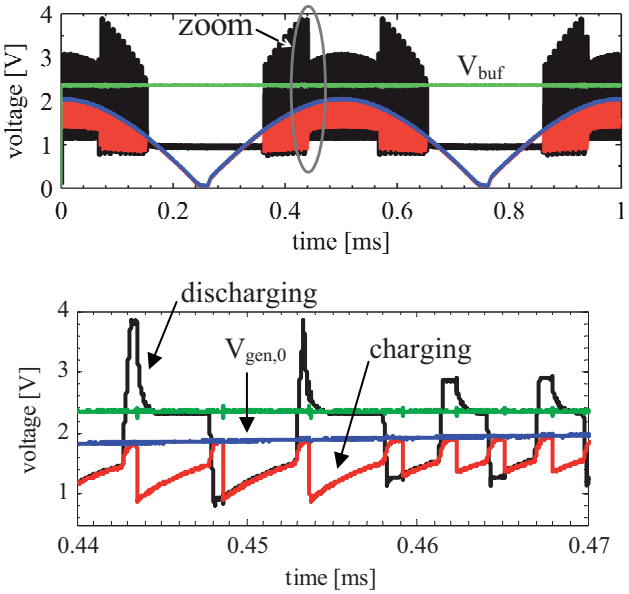

Fig. 5: Measured transient waveforms (a) of the impedance matching interface, also with zoom (b).

LOAD MATCHING DETECTOR

The detection of the optimal charge point for obtaining load matching is achieved by innovative sensing of current through a wide transistor M_{g3} (Fig. 7) of switch S_{gi3}. As the array capacitors get charged, the voltage across them as well as $V_{rect/2}$, rises while the charging current diminishes continuously. The amplifier (OTA) forces the current through M_{fb} to be exactly the current mirror fraction (M_{g3}:M_{g3}') of the actual generator current [4]. Thus, if resistor R_{sens} is sized in relation to the internal generator resistance R_{gen}, V_{sens} and $V_{rect/2}$ are equal in case V_{rect} equals 0.5 $V_{gen,0}$. Then, the comparator generates a transition of output signal V_{match}, as V_{sens} passes $V_{rect/2}$.This signal can then be used by the CCU to stop the charging of the capacitors.

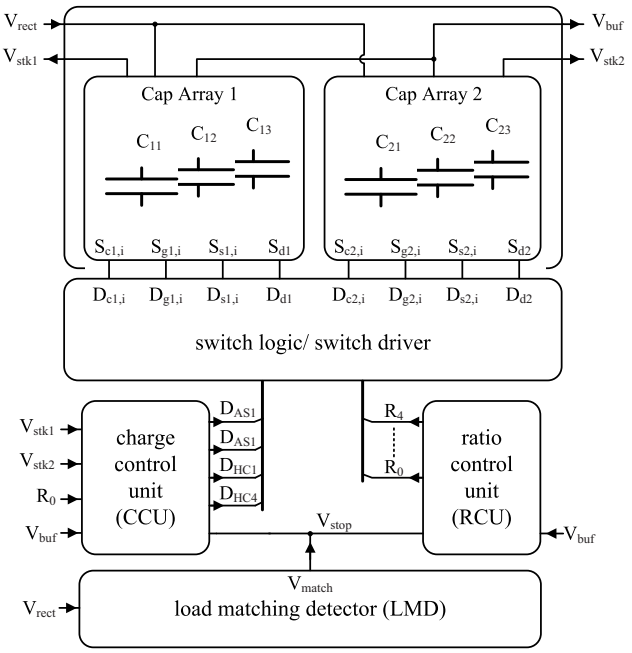

Fig. 6: Building blocks of the adaptive interface chip with added load matching detector.

Figure 8a shows the transient behavior over a rectified sine half-wave. Due to the cross coupled MOS transistors of the rectifier, there is no significant voltage drop across the rectifier [5].

Figure 8b reveals a delay between the $V_{rect/2}$ to V_{sens} equivalence and the comparator signal edge. This is due to limited comparator speed, and a build-in hysteresis. On the one hand, a minimum delay is essential, because otherwise fast successive switching events would cause high dynamic losses. On the other hand, a certain hysteresis will not affect the impedance matching significantly, because of a sufficient wide region where charging power is almost maximal [3]. Because of that adequate wide high power region, the sense resistor R_{sens} is practically sized to a higher value, so that V_{sens} equals $V_{rect/2}$ if V_{rect} is even at 60 % of the actual generator open-circuit voltage – instead of the 50 % where just the matching and power maximum is expected.

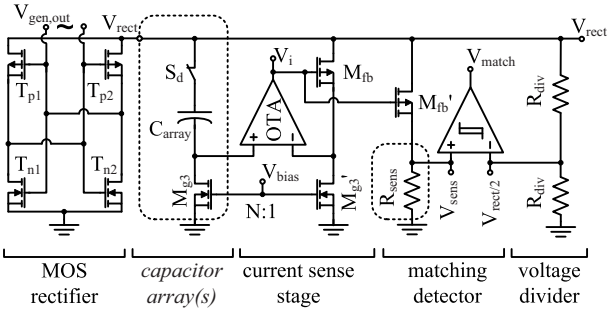

Fig. 7: Schematic shows load matching detector between the rectifier and array capacitors.

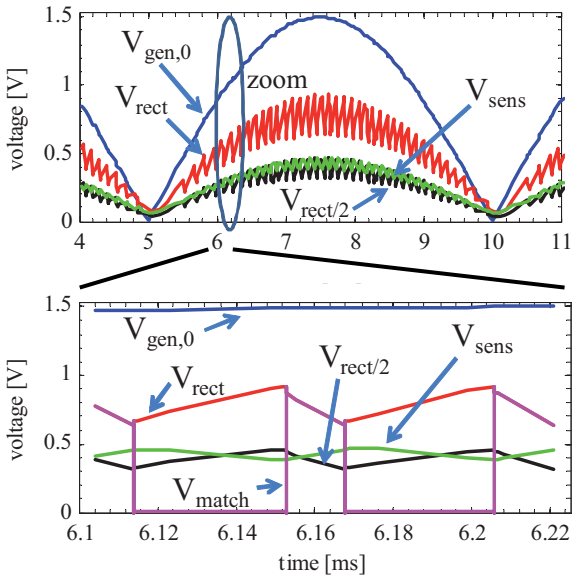

Fig. 8: (a) Simulations of the generator output voltage V_{gen} ($\approx V_{rect}$), which ripples around 1/2 $V_{gen,0}$, and (b) the zoomed view of the load matching detection – with delayed comparator signal V_{hc}.

The low dynamic requirements and weak inversion transistor operation allow supply voltages down to 0.4 V while power consumption is below 1.1 µW. At a maximum supply voltage of 3.3 V, the complete sense circuit dissipates less than 2.9 µW, because of supply independent biasing currents.

MEASUREMENTS AND DISCUSSION

The measurements are performed with a substitute of a typical generator for Figures 9 and 10, and with a real transducer (Fig. 3b) for comparisons (Fig. 11).

Using a transducer substitute was done for convenience of measurements, better reproducibility, and in order to acquire the open source generator voltage for calculating absolute maximum values. Therefore, the generator was substituted by a fully-differential sinusoid function generator and a series resistor R_{gen} (source resistance).

For evaluating the ability of impedance matching and voltage conversion two basic experiments are accomplished. First, the dependence of the generator output power to the capacitor charging state was measured. Therefore, the stop level of charging relatively to the actual open-circuit DC source voltage was stepwise increased. As Figure 9 shows, there is indeed a maximum of charging power at around 50-60 % of charging. Thereby, harvesting efficiency η_{hvst} is the charging power divided by the theoretical maximum available power. Hence, the charge control principle is a feasible method for obtaining impedance matching conditions.

A further focus was the gain due to voltage up-conversion with stacking of the array capacitors. This up-conversion allows harvesting even if the actual generator voltage is less than the buffer voltage. The dashed plots in Figure 10 show the maximum buffer voltage, e.g. at 1.5 V of generator voltage amplitude a final buffer voltage of around 2.4 – 2.6 V was measured in conjunction with a 100 kΩ load resistance. Such a light load was chosen in order to simulate a sleep state of a real autonomous system. The buffer gain factor expresses the factor of additional storable energy on a buffer capacitor, e.g. at that generator amplitude of 1.5 V the stored energy is around 2.5 times higher than without up-conversion.

Finally, a comparison between harvesting energy with and without the interface was done. The power source was an excited electro-dynamic transducer with 2.05 kΩ internal resistance and 168 Hz resonance frequency (Fig. 3b). The results in Figure 11 show that the generator output power depends typically on the load resistance if the interface chip is not used.

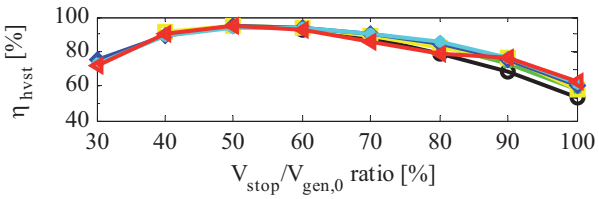

Fig. 9: The charging power and harvesting efficiency passes a maximum as charge stop level is increased.

However, if the interface chip is incorporated, the generator power remains almost constant as the load is swept. Due to switching gaps, switching losses, and a η_{hvst} of less than 100 % (90 – 95 % in Fig. 9), the peak power without the interface is higher. However, in a real system this certain load case may never or only very rarely occur. Due to the typical small duty cycle of autonomous systems it is more realistic that those systems apply load condition which equal either very low load resistances (active or transmitting mode) or very high load resistances (sleep mode).

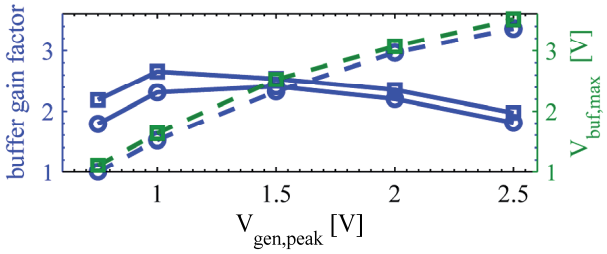

Fig. 10: Maximum buffer voltage due to stacking and resulting increase of buffered energy.

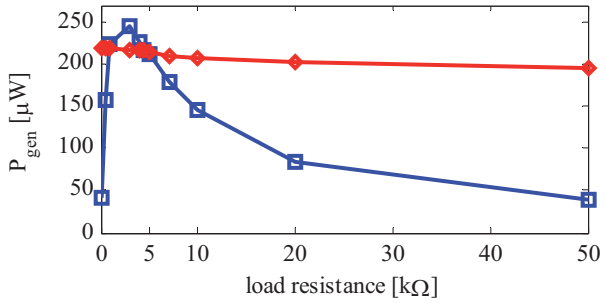

Fig. 11: Generator output power with (diamonds) and without (squares) the adaptive interface chip.

CONCLUSION

An interface chip for continuous impedance matching was presented in conjunction with a load matching detector. It is shown that the interface allows almost constant and high generator power at all load conditions. Beside the experimental prove of this charge controlled impedance matching method the integrated voltage up conversion allows storage of harvested power even at high buffer voltages. The presented load matching interface solves the fundamental problem of detecting the load matching point, with low power consumption only.

ACKNOWLEDGEMENT

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REFERENCES

[1] J.A. Paradiso, T. Starner "Energy scavenging for mobile and wireless electronics", IEEE Pervasive Computing, vol.4, no1., pp. 18-27, Jan-March 2005.

[2] E. Lefeuvre, A. Badel, C. Richard, L. Petit, and D. Guyomar, BA comparison between several vibration-powered piezoelectric generators for standalone systems,[Sensors Actuators A, Phys., vol. 126, no. 2, pp. 405–416, 2006.

[3] D. Maurath, M. Ortmanns, and Y. Manoli, High Efficiency, Low-Voltage and Self-Adjusting Charge Pump with Enhanced Impedance Matching, Proc. IEEE MWSCAS 2008, Knoxville, USA, Aug. 2008.

[4] T.Y. Man, P. Mok, and M.J. Chan, A 0.9-V Input Discontinuous-Conduction-Mode Boost Converter with CMOS-Control Rectifier, IEEE

[5] C.Peters, D. Spreemann, M. Ortmanns and Y. Manoli, A CMOS integrated voltage and power efficient AC/DC converter for energy harvesting applications, Journal of Micromechanics Microengineering, JMM, 18 104005, Issue 10, Oct. 2008.