DESIGN OF AN ASIC DEDICATED TO SSDI VIBRATION DAMPING

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Abstract: An ASIC implementing the non-linear Synchronized Switch Damping on an Inductor (SSDI) technique has been designed in a 0.35µm CMOS process with 50V high-voltage option (AMS H35B4D3). The ASIC integrates a high-voltage sensor interface and a low-voltage controlling part (including an envelope detector and a comparator). Coupled with piezoelectric patches, this circuit can be easily bonded on vibrating structures to damp mechanical vibrations. The presented system has two main functions. First, it performs a peak detection of piezoelectric output voltage to trigger high-voltage NMOS switching. Secondly, it allows a voltage reversing process by using an additional self and switching control. Its operation has been verified by damping tests on multi-modal structures.

Keywords: Synchronized switch damping, mechanical damping, electrical shunt, ASIC

INTRODUCTION

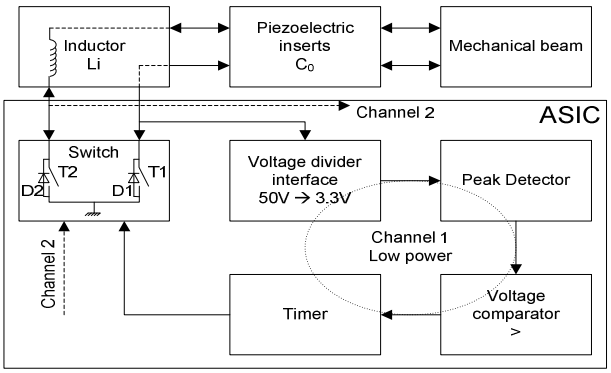
There have been different methods for vibration damping using piezoelectric inserts bonded on mechanical structures [1-2]. A semi-passive technique is called Synchronized Switch Damping (SSD) , which has a variant SSDI (SSD on an Inductor) [3]. SSDI technique is more efficient in terms of damping than strictly passive techniques [4].

Implementing the SSDI technique requires an electronic control circuit associated with piezoelectric inserts. The use of discrete components would decreases electromechanical coupling, and thus degrades damping efficiency. Circuit integration in microelectronic technology allows substantial reduction in mass and volume as well as circuit power dissipation. However, the needed inductance (typically hundred of micro-Henry) cannot be monolithically integrated. Thus a SMD inductor may be suggested.

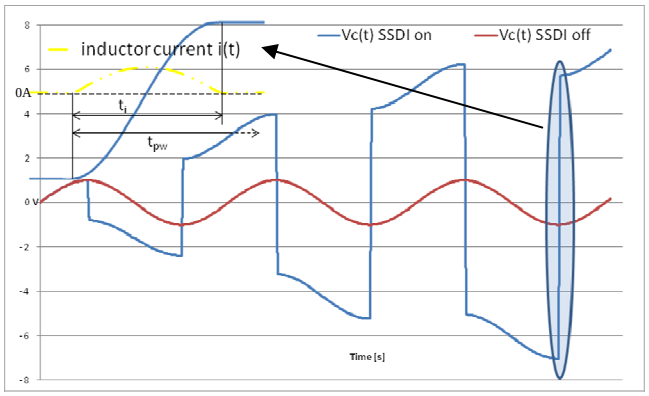
This paper presents an ASIC implementing the SSDI technique. It integrates sensing and controlling electronics apart from the SMD inductor. Our presentation includes circuit operation, optimal design and measured results.

CIRCUIT OPERATION

Fig. 1a shows the block diagram of the ASIC implementing the SSDI method. It is coupled with an external inductor L_i and piezoelectric inserts whose can be modeled by C_0 at the operating frequencies. The ASIC includes two identical nMOS switches T_1 and T_2 with paralleled by-pass diodes D_1 and D_2 to control the connection of the inserts with L_i. This forms an oscillating LC circuit when the instant voltage of the piezoelectric patch $V_c(t)$ reaches maximum or minimum, whose magnitude is denoted by V_0. At maximum values of $V_c(t)$, T_1 is switched on and D_1 is reverse biased, while T_2 is off but D_2 is forward biased. For minimum values, the operating states of these devices are reverse. The ASIC also includes two symmetrical channels made of a peak voltage detector to sense respectively maximum and minimum values of $V_c(t)$, and to drive a timer which controls switching states of T_1 and T_2. The timer generates a controlling pulse with pulse width t_{pw}, after which the patch is then disconnected (with both T_1 and T_2 switched off) until the next maximum or minimum of $V_c(t)$. This switching operation results in an "instant" quasi-inversion of $V_c(t)$, as shown in Fig. 1b. The inversion duration t_i corresponds to one short half pseudo-period of LC oscillation. It begins and ends when the LC circuit current goes to zero.



(a)



(b)

Fig. 1: a) ASIC functional diagram, b) SSDI non-linear processing.

OPTIMAL DESIGN

The goal is to design a generic ASIC compatible with the largest range of C_0 of inserts. An analytical model is then established to express C_0 acceptable values. This model is build from the *LC* circuit equivalent model during SSDI inversion. This allows identification of main parameters (shown in Table 2). Fig. 2 illustrates analysis of effects of the identified parameters. This analysis includes energy transfer optimization to ensure a high efficiency of SSDI non-linear treatment by minimizing energy loss during the inversion process. The effects of the main parameters are transcribed in design terms. For example, V_0 is a parameter and V_t is defined by process parameters. A C_0 range compatible with the identified constraints is given as a function of the switching transistors' channel width *W* and the inductor L_i. Such established relationships allow model computations by Matlab simulations. Fig. 3 shows the obtained design space for an initial voltage of 5V and a diode threshold voltage of 0.6V. The C_0 range is maximal for a maximal value of *W*. However we choose 1mm as a maximum value to limit the device surface area.

Table 1: Main parameters listing of the SSDI LC circuit equivalent model during voltage inversion.

E_0	Initial energy stored in C_0 before inversion
E_i	Final energy stored in C_0 after inversion
ΔE	Difference between E_0 and E_i
η	Energies yield
R_{on}	Switch transistor on-state resistance (T_1 or T_2)
R_{Li}	L_i inductor resistance
V_t	Switch diode threshold voltage (D_1 or D_2)
W	Switch transistor active gate length
I_{max}	Maximal peak current in *LC* serial circuit
V_{0m}	V_0 minimum value ensuring minimal η

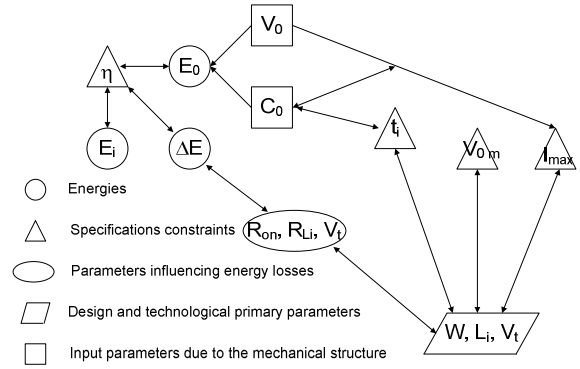


Fig. 2: Effects of main parameters.

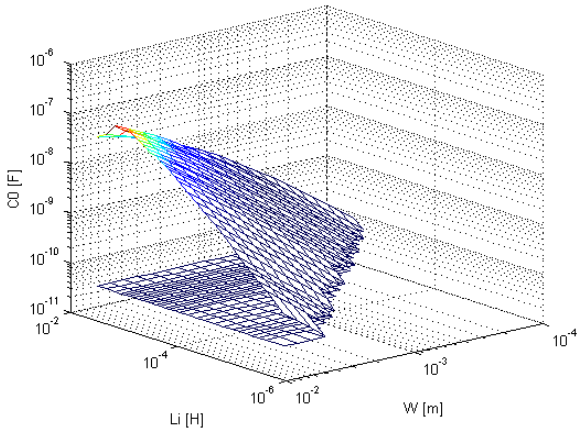


Fig. 3: Design space covering the C_0 allowable values in function of L_i and W for V_0 = 5V, V_t = 0,6V.

Although the chosen AustriaMicroSystems (AMS) 0.35µm H35B4 technology offers MOSFET components withstanding 50-V drain-source voltage, there are limitations of controlling signals to 3.3V. For sensing the piezoelectric patch voltage $V_c(t)$ that may reach a few ten volts, it is needed to insert a voltage divider before the sensing transistor's gate. Such a divider may provide several output voltage ranges for adaptation of the sensing transistor's gate. For a total number of ranges called *N*, a finite state machine, shown in Fig. 4, shows operation and transition of this generic divider.

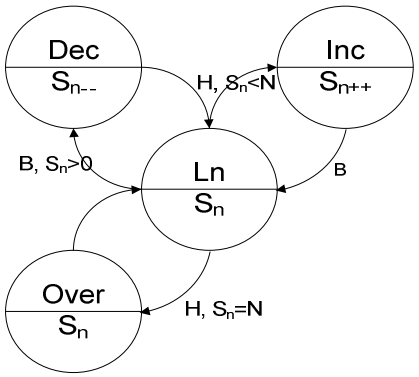


Fig. 4: Finite state machine of the voltage divider.

Transitions are automatically detected by measuring the output voltage V_s by means of two signals *H* and *B*. *H* indicates that V_s crosses a high threshold and *B* indicates a low threshold. L_n is the *nth* state among the *N* dividing level and S_n is the bit vector used to govern the *N* states. When *H* is active, S_n is decremented (*Dec* state) and incremented (*Inc* state) when *B* is active. An "*Over*" state is provided to protect the circuit in case of voltage overload. A voltage reverse is then unconditionally ordered to lower the input voltage by means of the yield η. We propose a capacitive voltage divider to limit electric charge loss due to the input signal low frequencies (<5 kHz). We implement a two range divider shown in Fig. 5. One range for a direct connection and the other for a dividing level called *m*. V_e input signal is applied on C_1 C_3 serial capacities and M_3 M_4 transistors ensure the dividing level selection. An R_{div} signal allows initialization of C_1 and C_3 if necessary.

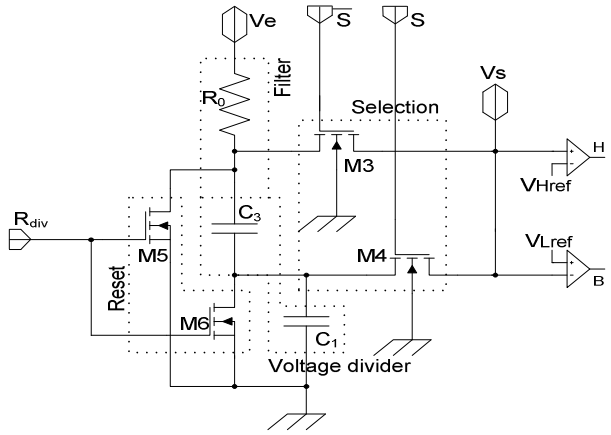


Fig. 5: Capacitive voltage divider implementation.

To avoid over voltage due to oscillation at the opening of the SSDI switch, we add a R_0 resistance at the input of the voltage divider. This forms a *RC* filter with C_1 and C_3. The junction capacitances C_{j1} and C_{j2} of the by-pass diodes D_1 or D_2 may be involved in parasite oscillations. D_1 and D_2 are implemented using the n-type drain and the p-substrate of T_1 and T_2 switching transistors. The oscillating pulsation of parasite oscillation ω_{par} is given by:

$$\omega_{par} = \frac{1}{2} \cdot \sqrt{\frac{4 \cdot L_i - r^2 \cdot C}{L_i^2 \cdot C}} \qquad (1)$$

Where *r* represents the Joule losses, *C* is an equivalent capacitance contributed by the patch capacitance C_0, the divider's capacitances C_1 and C_3, and the diodes' junction capacitances C_{j1} and C_{j2}.For a dividing level *m*, we have the transmittance (2):

$$\frac{V_s}{V_e} = \frac{\frac{C_3}{C_3 + C_1}}{1 + j\omega \cdot \frac{R_0 \cdot C_1 \cdot C_3}{C_1 + C_3}} = \frac{m}{1 + j\,\omega / \omega_c} \qquad (2)$$

To minimize effects of parasite oscillation, we choose the divider's capacitances C_1 and C_3, for the cutoff pulsation ω_c to equal $0.01 \cdot \omega_{par}$, with R_0 given by:

$$R_0 \geq \frac{C_1 + C_3}{C_1 \cdot C_3 \cdot \omega_c} \qquad (3)$$

It should be noted that the choice of C_1 and C_3 is also made with consideration of the divider's capacitive load C_{load}. To obtain C_1, $C_3 >> C_{load}$, we fix C_3 = 2pF and C_1 = 34pF. They are implemented in double poly-silicon.

RESULTS AND DISCUSSION

The fabricated prototype of the ASIC is shown in Fig. 6. Different functional blocks of the circuit have been tested. The main characteristics of the circuit are summarized in Table 2. To verify its operation, we have carried out damping tests on a beam structure as shown in Fig. 7.

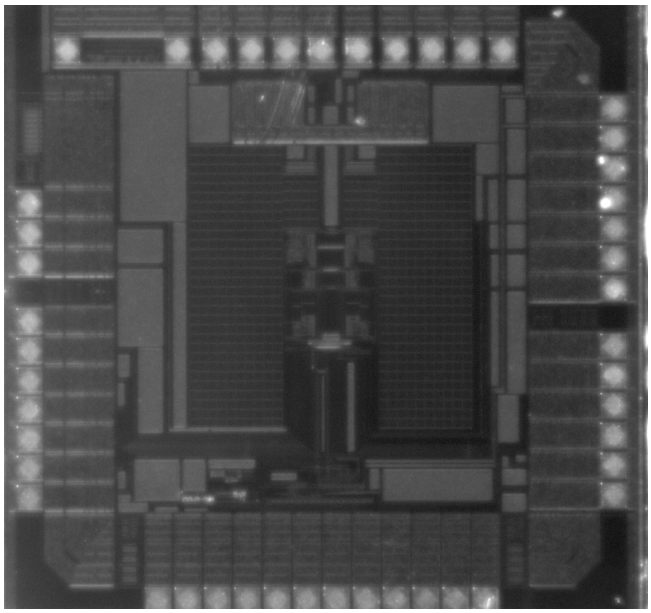


Fig. 6: Designed ASIC picture.

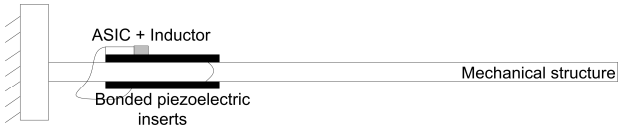


Fig. 7: Schematic of the electromechanical device.

Table 2: Main characteristics of the ASIC

Chip surface	2.5 *x* 2.5 mm^2
Voltage supply	$3.3V_{DC}$
Power dissipation	230µW*
Input voltage range (sensor)	0 – 50V
Low-voltage input voltage range	100m – 2.6V
Process technology	AMS H35B4
Pins (analogous – numerical)	46 (28 – 18)

*Simulated approximation

The test structure is a steel beam measuring 181.5mm *x* 94.5mm x 2mm with piezoelectric inserts bonded on each side. The piezoelectric material is PZT P189 and is located at 14mm from the clamped end. The sizes are 90mm *x* 40mm *x* 0.3 mm. The beam tip is submitted to a force F = 0,5N at 322Hz during 60ms. The first three measured resonance frequencies of the structure are 56.12Hz, 321,6Hz and 905.2Hz.

Fig. 8 shows waveforms of $V_c(t)$ with and without SSDI control (i.e. ASIC on and off). It can be seen that the ASIC performs maximum and minimum detection as well as inversion process. We can also observe a "rebound" at the end of inversion, which degrades voltage inversion efficiency.

Fig. 9 shows the measured spectra of mechanical vibration of the beam tip *u(t)*. The obtained results exhibit only two main flexional modes 1 and 2 with and without SSDI. They are respectively at 56Hz and 322Hz. The estimated damping is 3.1dB for the first mode and 1.7dB for the second one.

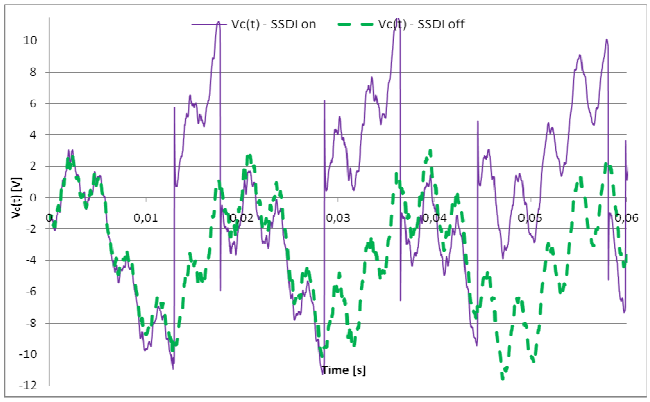


Fig. 8: Piezoelectric voltage $V_c(t)$ with and without SSDI control.

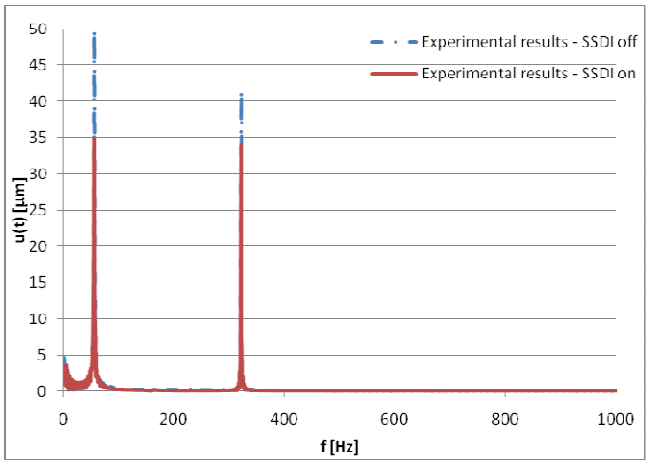


Fig. 9: Measured spectra of mechanical vibration for SSDI ASIC on and off state.

CONCLUSION

We have designed an ASIC implementing the SSDI technique. It integrates high-voltage sensor interface and low-voltage control functions. It is dedicated to operation with coupled piezoelectric inserts and an external SMD inductor. Multi-modal damping tests have been carried out to verify its operation. The estimated damping is 3.1dB for the first mode and 1.7dB for the second one.

ACKNOLEDGEMENTS

This work is funded by the French "Direction Générale pour l'Armement" with an Innovation Exploratory Research project (REI).

REFERENCES

[1] Belloli A, Niederberger D, Pietrzko S, Morari M, Ermanni P 2007 Structural vibration control via r-l shunted active fiber composites *J. of intelligent material systems and structures* **18 275 - 287**

[2] Qiu Z C, Zhang X M, Wu H X, Zhang H H 2007 Optimal placement and active vibration control for piezoelectric smart flexible cantilever plate *J. of sound and vibration* **301 521-543**

[3] Guyomar D, Richard C 2005 Non-linear and hysteretic processing of piezoelement: application to vibration control, wave control and energy harvesting *Int. j. of applied electromagnetics and mechanics* **21 193-207**

[4] Corr L R, Clark W W 2002 Comparison of low-frequency piezoelectric switching shunt techniques for structural damping *Smart materials & structures* **11 370-376**