

A MONOLITHIC CAPACITIVE DC-DC CONVERTER FOR A LOW VOLTAGE ENERGY SCAVENGING APPLICATION: ANALYSIS AND MEASUREMENTS

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Abstract: This paper analyzes the use of a monolithic DC-DC converter in a battery less energy scavenging application. A capacitive DC-DC converter is fabricated in CMOS 90 nm technology and a test bench is built to demonstrate the performance of the converter in a typical application. A model for the converter under varying input voltage is developed and used to predict the converters behavior.

Keywords: Monolithic, DC-DC converter, 90nm CMOS

1. INTRODUCTION

Over the last decade the interest in ubiquitous intelligence has grown rapidly. RFID tags found their first commercial applications and various variants of sensor networks are being developed at numerous research facilities over the world. A lot of research effort has been directed towards energy scavenging and making the network independent from batteries or other finite energy sources.

This can be achieved by means of different types of energy scavengers, ranging from thermo-electric solutions to mechanical scavengers. It is however appealing to implement the energy scavenger in the same technology as the digital circuits. This way a very compact and robust solution is suggested. These digital circuits: transmitters, receivers and control logic, are implemented in bulk CMOS technology. In [1] it is shown that radio frequency energy can be extracted from the environment. This is done by means of an on-chip antenna and an on-chip AC-DC converter. The scavenged energy is stored as charge on a capacitor and addressed when necessary. Since it has turnout either difficult or time consuming to scavenge energy from the environment, it is of primary concern for the system designer to benefit as much as possible from the actual gathered energy amount.

This paper investigates the use of a monolithic capacitive DC-DC converter in an energy scavenging application. First the approach is introduced in Section 2 and the system is presented in Section 3. Next the converter and a model of the converter are presented for the converter subject to a varying input voltage in Section 4. Finally a measurement setup is proposed and the measurements are presented in Section 5.

2. APPROACH

Thanks to voltage scaling, the power consumption in digital circuits can be reduced significantly. Because of that, it is interesting from a power consumption point of view to reduce the actual supply voltage of the circuit by putting a linear regulator between the supply and the load. This is shown in Fig 1 a). Not only will this reduce the power consumption, this regulator also derives a stable voltage from the storage capacitor. The

capacitor voltage is actually decreasing due to the current load.

A linear regulator achieves a first power reduction by means of reducing the voltage swing of the digital circuits but is on the other hand inefficient, since the excess voltage is dissipated in the regulators pass device.

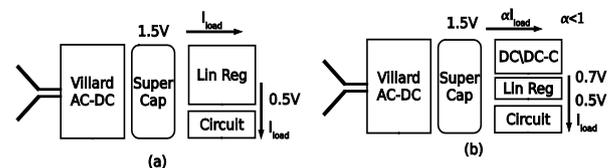


Fig. :1 a) Use of a Linear regulator b) Use of a DC-DC converter in a system with a regulated supply.

By means of replacing the regulator by a DC-DC converter (shown in Fig. 1 b)), the systems efficiency is increased and the current drawn from the capacitor is reduced. This increases the system's lifetime and introduces an increase in the overall power efficiency of the system. The monolithic integration of DC-DC converters is still quite cumbersome. The traditional implementations, using an inductor, suffer a lot from the low quality of the integrated inductors [2]. Therefore they achieve rather low efficiencies which makes it hard to compete with linear regulators. Recently however interest in DC-DC converters, using nothing but capacitors and switches has grown. And these converters have proven to achieve high efficiencies (>80%) [3] [4]. This makes them interesting for this kind of applications.

3. SYSTEM

In Fig. 1 the system is shown. A Super Capacitor is used as an energy reservoir. During operation, current is drawn from the capacitor and the supply voltage decreases linearly (shown in Fig. 2). Without a DC-DC converter, the current drawn from the capacitor equals the load current. At a certain voltage V_x at which the regulator shuts down, the operation is halted. So the operation period is determined by the voltage V_x , the maximum capacitor voltage $V_{cap,max}$ the load current and the capacitor size. $V_{cap,max}$ is determined by the maximum allowed voltage of the CMOS technology, the capacitor size is determined by the size and the cost of the component, V_x is

determined by the desirable output voltage of the circuits and the dropout voltage of the linear regulator.

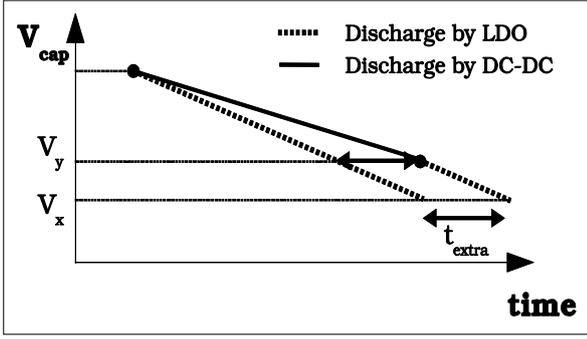


Fig. 2: Discharge diagram of a capacitor under different loads in function of time.

Adding a DC-DC converter is most of all beneficial for the upper part of the input voltage range. Once the input voltage drops beyond V_y the converter will be unable to maintain the wanted output voltage due to fundamental limitations of this type of converter.

This work focuses on the implementation of a monolithic DC-DC converter (Section 4) and the potential increase in overall power efficiency (Section V).

4. DC-DC CONVERTER

The converter is a 4/5-converter. It operates by switching between two configurations (shown in Fig. 3). While switching between these configurations charge is transferred from the input to the load. It has an ideal voltage conversion ratio of 0.8. Capacitive converters are however not lossless and have even in an ideal implementation a non-zero output impedance. The output impedance is described in Eq. 1. In this equation f_s is the switching frequency, C_{tot} is the total amount of capacitance and K_c a topology constant. The model of a capacitive DC-DC converter is represented in Fig. 4. The finite output impedance introduces losses which are called intrinsic losses since they are related to the fundamental characteristics of this type of capacitive DC/DC-conversion (Eq. 2). Next to the intrinsic losses there are also extrinsic losses (Eq. 3). The latter are related to the implementation characteristics of the converter. Namely the capacitive switching losses introduced by the energy that is necessary to switch the CMOS transistors. Equation 4 describes that the total output power is a function of the output voltage and output current.

$$R_{out} = \frac{K_c}{C_{Tot} f_s} \quad (1)$$

$$P_{loss, intr} = (NV_{in} - V_{out}) I_{out} \quad (2)$$

$$P_{loss, extr} = f_s \sum_i (V_{swing,i}^2 C_{gate,i}) \quad (3)$$

$$P_{out} = V_{out} I_{out} \quad (4)$$

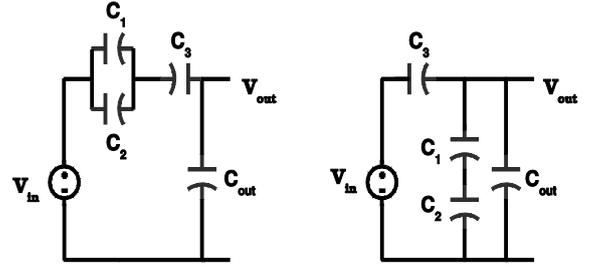


Fig. 3: Converter Topology: 4/5 fractional converter

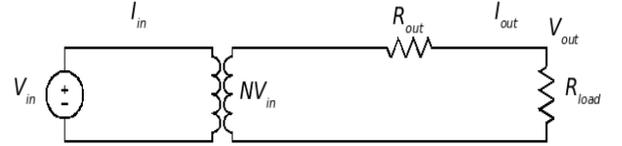


Fig. 4: Converter Output Impedance Model

The overall efficiency η is given in Eq. 5. It is clear from Eq. 6 that the current, drawn from the input, is inverse proportional to the converters efficiency. In case of constant current load and constant output voltage, only the input voltage and related efficiency determines the current drawn from the input voltage source.

$$\eta = \frac{V_{out} I_{out}}{V_{in} I_{in}} \quad (5)$$

$$I_{in} = \frac{V_{out} I_{out}}{\eta V_{in}} \quad (6)$$

In Eq. 7 the definition of γ is introduced and the output impedance model makes clear that V_{out} can be represented as a result of a voltage division between an output resistance and the equivalent load resistance (Eq. 8). Equation 9 demonstrates that an increase in input voltage results in a proportional decrease in γ . While γ determines the intrinsic losses and thus influences the overall efficiency negatively. On the other hand will this decrease in γ give raise to an increase in output impedance to maintain constant output voltage. This increasing output impedance reflects in a decreasing switching frequency and thus lower extrinsic losses. The latter positively influencing the overall efficiency.

$$\gamma = \frac{V_{out}}{NV_{in}} \quad (7)$$

$$V_{out} = \frac{R_L}{R_L + R_{out}} NV_{in} \quad (8)$$

$$V_{out} = \gamma_{max} NV_{in} \quad (9)$$

If V_{in} is higher thus $V_{in}^{new} = KV_{in}$ with $K > 1$

$$\gamma_{\max}^{\text{new}} = \frac{\gamma_{\max}}{K} \quad (10)$$

Eq. 10 can be expanded by substituting Eq. 8. This gives us Eq. 11 which is solved towards the new output impedance under effect of the increase of voltage in Eq. 12. K_{R0} depicts the effect on the output impedance of an increase in input voltage with a factor K . Equation 14 shows that K_{R0} is a function of the factor K , the initial output impedance and the equivalent load resistance which is constant.

$$\frac{R_L}{R_L + R_{out}} NV_{in} = K \frac{R_L}{R_L + R_{out}^{\text{new}}} NV_{in} \quad (11)$$

$$R_{out}^{\text{new}} = KR_{out} + (K-1)R_L \quad (12)$$

$$K_{R0} = \frac{R_{out}^{\text{new}}}{R_{out}} \quad (13)$$

$$K_{R0} = K + (K-1) \frac{R_L}{R_{out}} \quad (14)$$

In order to quantify the impact of an input voltage back off on the overall efficiency, Eq. 15 is evaluated. By substitution of Eq. 7, Eq. 4 and introducing β , the ratio between the extrinsic losses and the output power, a modified definition of the converter's efficiency is given in Eq. 17.

$$\eta = \frac{P_{out}}{P_{in}} \quad (15)$$

$$\eta = \frac{P_{out}}{P_{out} + P_{loss,ext} + P_{loss,int}} NV_{in} \quad (16)$$

$$\eta = \frac{1}{1 + \frac{1-\gamma}{\gamma} + \beta} \quad (17)$$

Thus if an input voltage back off of K appears the resulting efficiency is given by:

$$\eta_{\text{new}} = \frac{1}{\frac{K}{\gamma} + \frac{\beta}{K + (K-1) \frac{R_L}{R_{out}}}} \quad (18)$$

$$\frac{\eta}{\eta_{\text{new}}} = K + \frac{\beta\gamma}{K + (K-1) \frac{R_L}{R_{out}}} \quad (19)$$

In Eq. 6 it was shown that, for a fixed load voltage and current, the input current of the DC-DC converter is a function of the input voltage and the converters efficiency. The latter being a function of the input

voltage.

In order to simulate the effect of inserting a DC-DC converter in the system, the current consumption of the DC-DC converter is calculated.

With help of the presented equations a numerical discrete time analysis is performed on the system and the efficiency improvement of the system can be calculated. In Fig. 5 a print out of the transient behavior is shown. It is clear that adding a DC-DC converter has the potential of increasing the operation period significantly. These results are validated by means of the measurements in the next section.

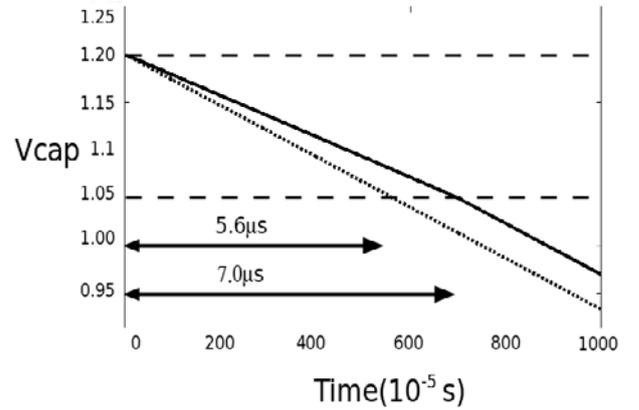


Fig. 5: Discharge Diagram with MATLAB model

5. MEASUREMENTS

A test bench (Fig. 6 and Fig. 10) has been setup consisting of a periodic charger emulating the AC-DC conversion and a capacitor of 40nF. In a first test the capacitor has been loaded with a constant current load of 1mA. This Gives us the discharge rate in case a linear regulator would be used for this purpose. In a second case the DC-DC converter has been inserted for improving overall system efficiency. The DC-DC converter has been loaded with a constant current load of 1mA as well and keeps the voltage constant at 675mV.

The measurements were performed with the test bench described in the previous paragraph. The capacitor is charged to 1.19V and then discharged by the constant current load. First without inserting the DC-DC converter and next after inserting the presented converter. In Fig. 7 the output voltage is shown under constant current load. In Fig. 8 the output voltage is when the DC-DC converter is inserted. It is clear that for an output voltage of 1.05V the capacitor discharge time is extended with 24% from 5.64μs to 7μs. This leads to a significant increase in lifetime of the application. In fact this increase in lifetime can be exploited to reduce the energy scavenging requirements for example reducing the antenna or capacitor size.

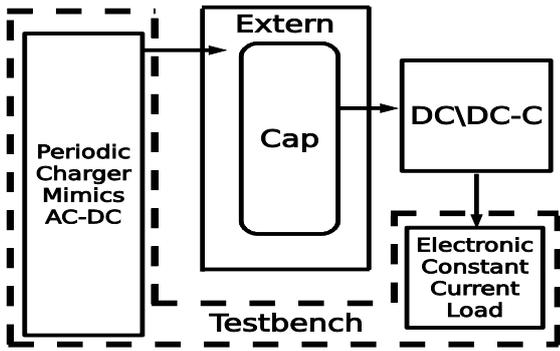


Fig. 6: Schematic of the Test Bench

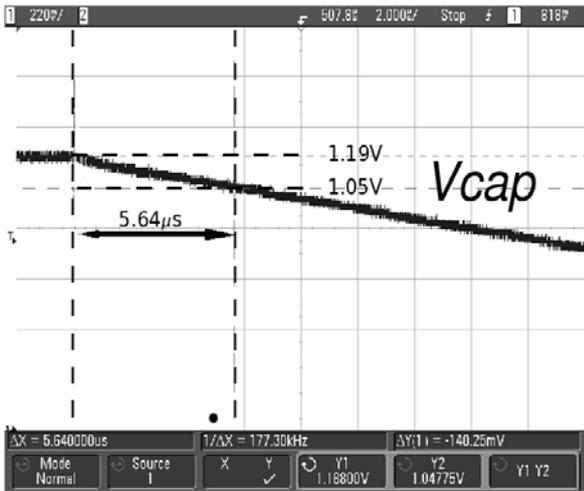


Fig. 7: In circuit Test without DC-DC converter

CONCLUSION

It has been demonstrated that using a monolithic DC-DC converter in a battery less application increases the application's lifetime significantly. A model has been proposed for predicting the system performance based on a limited number of parameters. This model was used in a MATLAB simulation and fits the measurements results closely. A Test bench has been used for mimicking the system behavior and demonstrating the DC-DC converters potential under realistic circumstances.

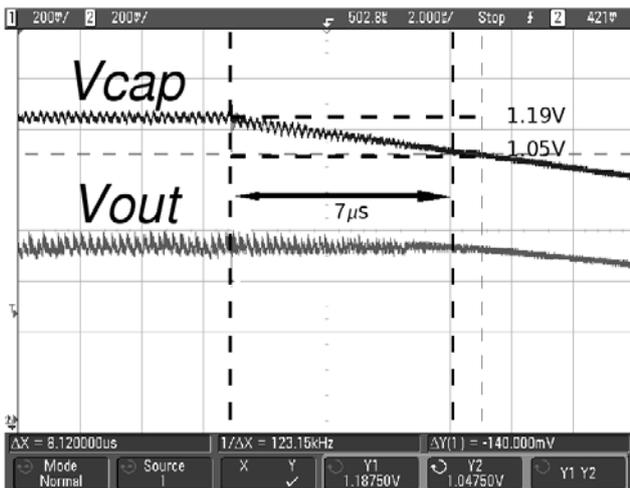


Fig. 8: In circuit Test with DC-DC converter

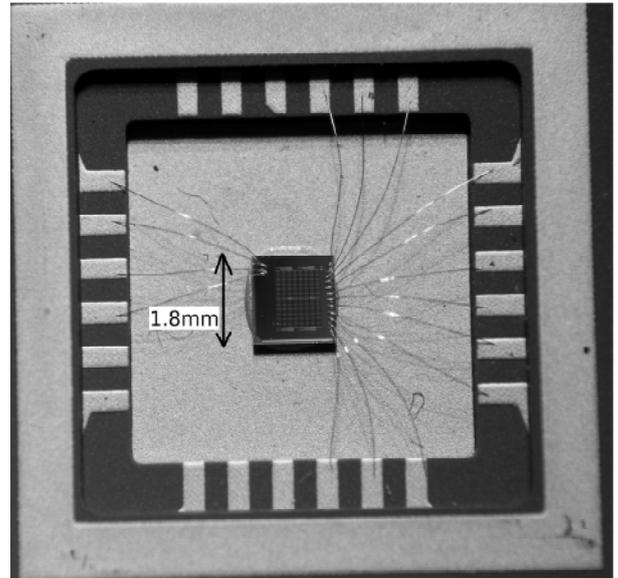


Fig. 9: Photograph of the die



Fig. 10: PCB realization of the Test Bench

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