A DIGITALLY ADJUSTED POWER SUPPLY FOR SYSTEMS-ON-CHIP BASED ON CMOS INTEGRATED FUEL CELLS

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Abstract: This paper presents the design and measurement results of a versatile on-chip power supply implemented as a CMOS-integrated fuel cell (FC) array with a digitally selectable output voltage. Using an adjustable low drop-out voltage regulator (LDO) and an adaptive FC arrangement the user-selectable output voltage is stabilized to 1.1 V, 1.3 V, 1.8 V, 2.2 V, 2.6 V or 3.3 V. Furthermore, the 3 different FC arrangements increase the power efficiency by decreasing the LDO voltage drop for lower output voltages. The system is fully implemented on-chip in an extended 0.45 µm automotive CMOS process. The maximum quiescent and output current of the voltage regulator is measured to be 1.74 µA and 225 µA, respectively.

Keywords: Voltage Regulator, LDO, SoC, Fuel Cell, Power Supply, Chip Integrated Fuel Cells

INTRODUCTION

A main challenge in systems-on-chip (SoC) is their power supply. While transistor sizes scale down with process development batteries do not scale in the same rate. Various SoCs were developed recently, which include e.g. voltage regulators and sensors [1-4], but still require for an external power supply. In contrast to these, a CMOS system including the power source without the need for external components like batteries, coils or capacitors is presented in [5].

The presented system here improves the one from [5] by providing various different output voltages allowing different modes of operation with its specific voltage demands like low, mid or high voltage for e.g. standby, data acquisition or data transmission mode, respectively, while voltage efficiency is increased by up to 57% by adapting the fuel cell connections.

SYSTEM OVERVIEW

A system overview is shown in Fig. 1. It comprises a core circuit, an on-chip FC array and a voltage regulator. No external components like capacitors, batteries or inductors are needed. The connections of FCs in the array can be varied allowing for a variable output voltage. This array powers the voltage regulator with its two amplifiers and the connected load. In the reference adjustment circuit (RAC) of the voltage regulator a low-speed operational amplifier (OP) in combination with its variable feedback is responsible for the fine adjustment of the reference voltage. The high-speed error amplifier (EA) of the output voltage controller (OVC) with its feedback controls the output voltage via the pass transistor M_{pass}. Configured by 3 digital input pins ("select V_{out}") the core circuit controls the LDO feedback, the RAC feedback as well as the fuel cell connection. Additionally, the core circuit generates the reference voltage for the RAC and bias currents for the OP and the EA.

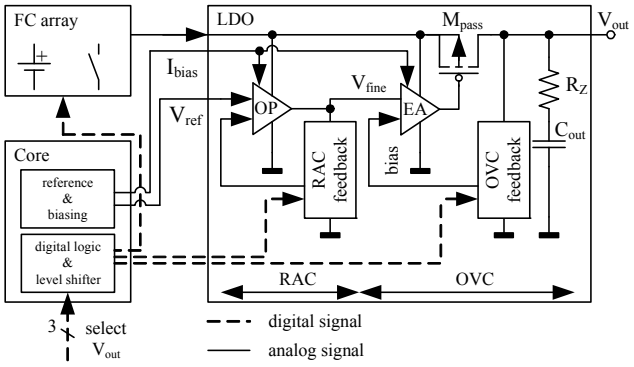

Figure 1: System overview including fuel cell (FC) array, core circuit with reference voltage and LDO.

FUEL CELL ARRAY

The chip includes 42 fuel cells grouped as 6 single FCs, 6 cathode connected stacks (CCS), and 6 anode connected stacks (ACS). Each stack contains 3 FCs in series, as shown in Fig. 2(a). Four additional FCs permanently power the core as described in [5]. The normalized characteristic of a single FC is shown in Fig. 3 [5]. With the targeted area per FC of $A_{FC} = 1\ mm^2$ this results in a maximum output power per FC of $P_{max} \approx 4.50\ \mu W$.

To power the load, 3 FC configurations are possible to build parallel fuel cell cascades (FCCs). 7 FCs in a series connection, build by 1 ACS, 1 CCS and 1 single FC in between, result in 6 parallel FCCs (Fig. 2(b)). 6 FCs in series, assembled by 1 ACS, 1 CCS and the 6 single FCs forming an extra cascade, lead to 7 parallel FCCs (Fig. 2(c)). A series connection of 3 FCs is formed by each ACS and each CCS while two additional FCCs are build up with the 6 single FCs resulting in 14 FCCs in parallel (Fig. 2(d)). These 3 FC configurations, the selectable 6 output voltages and the estimated maximum system output current and power are listed in Table 1. The reduction of the LDO input

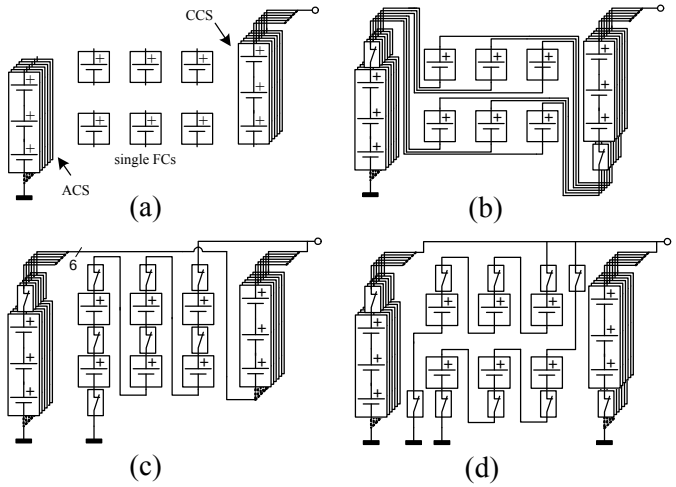

Figure 2: On-chip controlled FC arrangement (a) with 7 (b), 6 (c) and 3 (d) FCs connected in series with 6, 7 and 14 FC stacks in parallel, respectively.

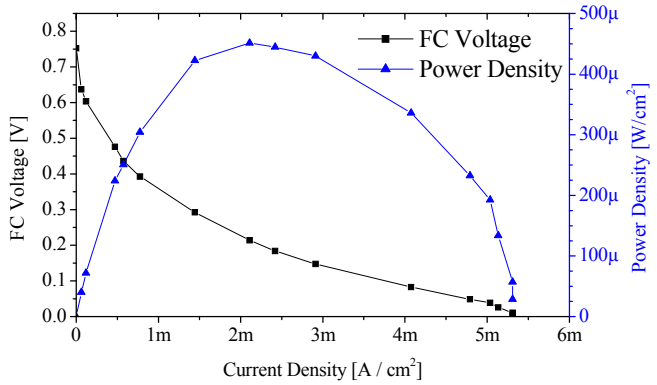

Figure 3: Output characteristic of the chip-integrated FCs [5].

voltage by adapting the height of the fuel cell stacks to the desired output voltage improves the voltage efficiency by up to 57% compared to a fixed connection of 7 FCs in series.

The variable connection of FCCs is attained with MOS transistors controlled by the core circuit. Depending on the switch position, either PMOS or NMOS transistors are used. The circuits for controlling the NMOS and PMOS switches are shown in Fig. 4(a) and Fig. 4(b), respectively. The level shifter (LVL-Shifter) in Fig. 4(a) increases the input signal from the core voltage level (1.1 V – 1.5 V) to the FC array voltage. The PMOS switch in Fig. 4(b) works accordingly but with inverted signals. The added cross coupled transistors in Fig. 4(b), M_{b1} and M_{b2}, prevent the parasitic diodes between source or drain to the well from being forward biased.

VOLTAGE REGULATOR

The voltage is stabilized by an LDO. Its principle is shown in Fig. 1 and explained in [6]. A voltage reference implemented in the core circuitry [5] delivering $V_{ref} = 340$ mV is used for output voltage regulation. The OVC feedback is implemented with diode connected PMOS transistors as voltage dividers. To divide the voltage consistently for all 6 output voltages and independent of process variations these

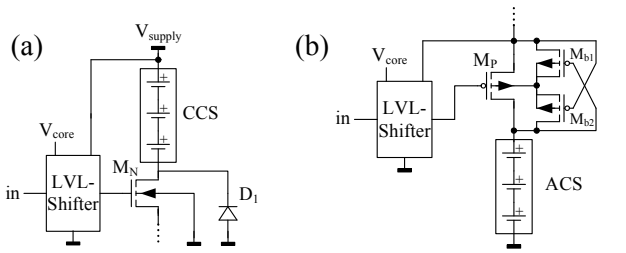

Figure 4: Switches including level shifter to achieve bootstrap switching and diodes to prevent the parasitic diodes from being forward biased.

transistors have to be dimensioned and biased equally. Hence, with a threshold voltage of $V_{th} \approx 900$ mV–1.1 V and the targeted output voltages from 1.1 V up to 3.3 V this only allows for a voltage division by 2 or 3. A resistive feedback in this case is not advisable. With currents of a few hundreds of nA at $V_{out} = 3.3$ V the resistors would be in the range of 10s of MΩ leading to excessive use of chip area. Additionally, due to their parasitic capacitances these high value resistors would form a low frequency pole in the feedback path. A decreased load regulation and stability of the system would be the result. The schematic of the OVC's error amplifier is shown in Fig. 5(a). It comprises an NMOS input stage (M_{1A}, M_{1B}, M_{2A}, M_{2B}, M_{3A}) and a second gain stage (M_{3B}, M_4) driving the PMOS pass element M_{pass} in Fig. 1. By inserting an additional zero at the output with $C_{out} = 600$ pF and the addition of resistor $R_Z = 6$ kΩ stability was achieved over the whole input and output voltage range of the FCs and the LDO.

The RAC as shown in Fig. 1 utilizes a weak-inversion operational amplifier (OP), configured as non-inverting amplifier with switchable resistive feedback. A resistive feedback can be applied here due to the fact, that only low-voltage DC signals are amplified and a constant load is applied at the output. The schematic of the OP is shown in Fig. 5(b). It is a two stage Miller compensated amplifier topology with a PMOS input stage (M_{5A}, M_{5B}, M_{6A}, M_{6B}, M_{9A}), a second gain stage (M_7, M_{9B}) and a source follower buffer stage (M_8, M_{9C}). Simulations show a gain bandwidth product of $GBW = 12.47$ kHz with a DC gain of $A_{DC} = 67.1$ dB and a typical phase margin of $PM \approx 73°$.

Table 1: Measured quiescent and output current of the LDO ($I_{q,LDO}$, $I_{max,LDO}$) and the predicted maximum fuel cell current ($I_{max,out}$) and system output power $P_{max,out}$ with n FCs in series and m parallel FCCs for all selectable output voltages (V_{out}).

V_{out} [V]	$I_{q,LDO}$ [µA]	$I_{max,LDO}$ [µA]	$I_{max,out}$ [µA]	$P_{max,out}$ [µW]	n	m
1.1	1.51	185	130	143.0	3	14
1.3	1.32	131	83	107.0	3	14
1.8	1.58	225	96	172.8	6	7
2.2	1.74	220	73	153.3	6	7
2.6	1.32	130	55	143	7	6
3.3	1.58	166	28	92.4	7	6

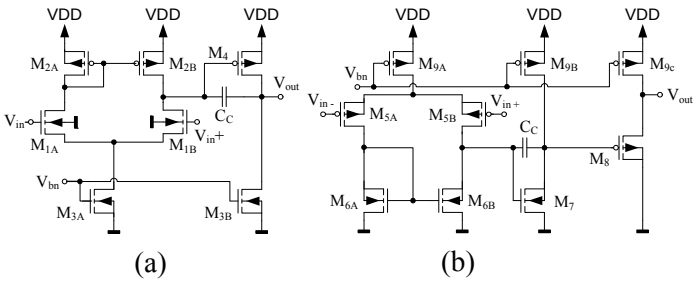

Figure 5: Schematic of the error amplifier used in the OVC (a) and the weak inversion amplifier employed in the RAC (b).

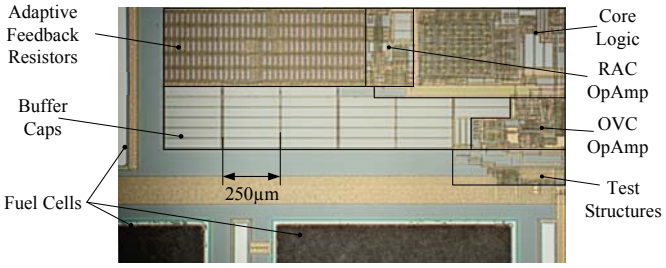

Figure 6: Chip micrograph of the electronic part of the proposed adjustable on-chip power supply. Parts of the 42 fuel cells can be seen around this block.

The feedback of the RAC and the OVC can be switched in three steps each, enabling 6 different feasible output voltages. The selection of the feedbacks is done via 3 digital input pins ("select V_{out}"). This allows an output voltage in the range from $V_{out} = 1.1$ V to $V_{out} = 3.3$ V.

MEASUREMENT RESULTS

The proposed system is implemented in an extended 0.45 µm automotive CMOS process. A chip micrograph is shown in Fig. 6. The area of the RAC and the OVC with the digital control circuits and the output capacitor is approximately 350×1130 µm^2 and 280×1800 µm^2, respectively.

CURRENT CONSUMPTION

The proposed voltage regulator architecture with its measured current consumption of $I_{q,LDO} \leq 1.74$ µA enabled a power reduction by up to 69% when compared to [5]. This current consumption is 18% lower than simulations predicted. The main deviations originate from a shift in the resistance in the biasing network. Test structures on the chips exhibit resistor values of 1.5 times the nominal value with a standard deviation of $\sigma \approx 6.9\%$, indicating a systematic error. Simulations of the quiescent current with 1.5 times the nominal resistor values are – despite chip-to-chip variations – in good agreement with the measurements as shown in Fig. 7. Further analysis of simulation and measurement mismatch are based on the drain current of a current mirror biased in the core and mirrored to a test pad. These measurements show a good agreement between the measured mean current and the simulated mean current with a resistance deviation of +50% to +70%.

Due to the large FC area, the design rules of more than 30% coverage with metal, poly and diffusion layers are not met, resulting in e.g. adjusted etching parameters. Additionally hydrogen treatment during the FC charging may have a significant influence on the behavior of the electronic devices. Possible effects are not yet analyzed. Despite the measured deviations, the robust design of the circuits yields a fully functional system as shown in the following subsections.

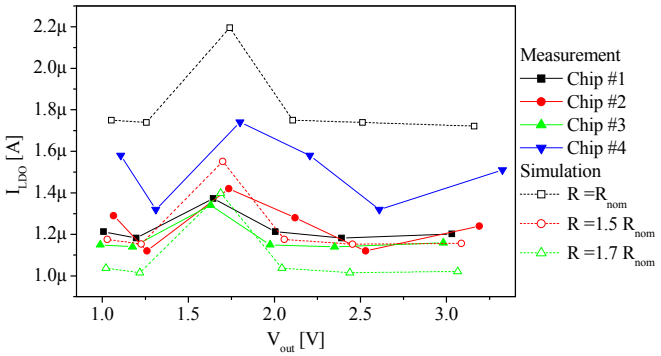

Figure 7: Quiescent current of the LDO at the measured output voltages in comparison to the simulated values. It can be seen that the measurements match to a resistance of $R = 1.5\ R_{nom}$.

LINE REGULATION

The output voltage can be varied in 6 steps from $V_{out} = 1.1$ V up to $V_{out} = 3.3$ V. Except negligible random variations, the output voltage is regulated to a constant value depending on the output voltage selection. As shown in Fig. 8 the LDO output voltage V_{out} is independent of its input voltage V_{in} e.g. the fuel cell cascade voltage. For the two lowest output voltages of $V_{out} = 1.1$ V and $V_{out} = 1.3$ V, the output voltage is increased by $V_{out} \leq 170$ mV at very low input voltages. In this operation region, the input swing of the LDO EA is not sufficiently high to fully turn off the pass transistor.

LOAD REGULATION

Fig. 9 shows the load regulation of the voltage regulator and the characteristics of the FCs from [5] connected as stacks as described in subsection FUEL CELL ARRAY. The maximum allowed output current of the LDO for a guaranteed constant output voltage is larger than the maximum current delivered by the FCs for all configurations. Thus, future FCs with improved current characteristics can be applied to the voltage regulator without any modifications. Aforementioned process variation leads to variation of the output voltage V_{out} as shown in Fig. 7-10. The maximum deviation to the ideal value in Fig. 9 is + 90 mV at $V_{out} = 1.3$ V corresponding to a deviation of + 6.9%.

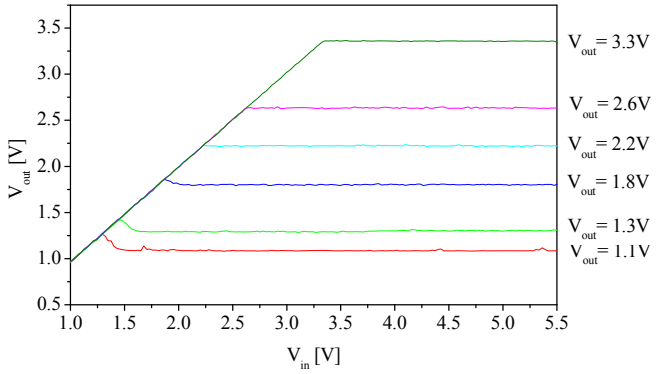

Figure 8: Measured line regulation of the system with a resistive load of R_{load} =1 MΩ.

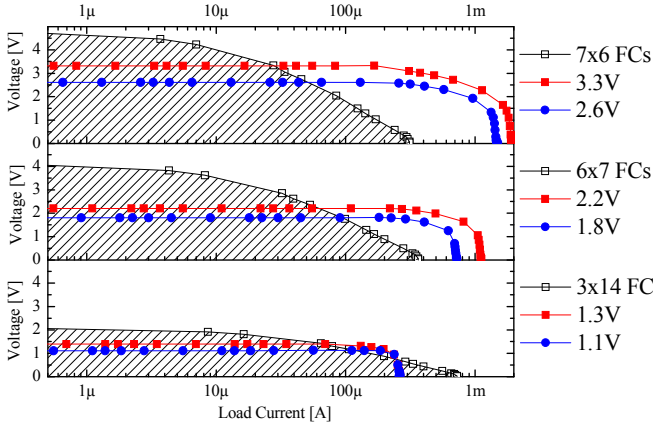

Figure 9: FC stack characteristics and the measured load regulation of the LDO at three different FC stack connections.

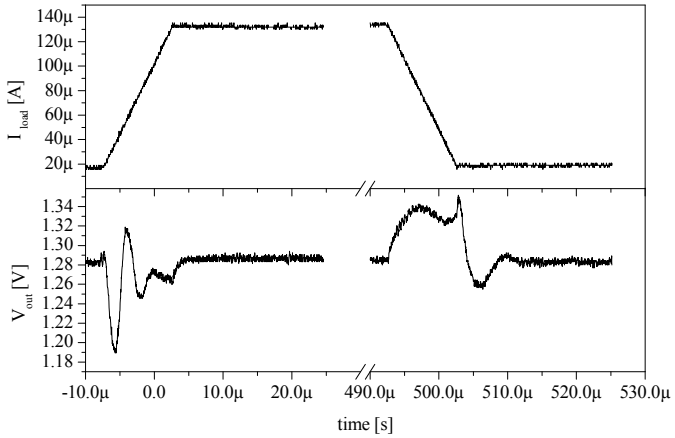

Figure 10: Typical step response of the LDO measured for an output voltage of 1.3 V at a supply voltage of 1.5 V and a rise and fall time of 10 µs.

STEP RESPONSE

The stability of the voltage regulator is proven by step response measurements. Fig. 10 shows a measured exemplary step response at an output voltage of V_{out} = 1.3 V. The graph shows little ringing at a load step form $I_{load} \approx 17$ µA to $I_{load} \approx 132$ µA. Even under these harsch load conditions the stability can be guaranteed.

SUMMARY

In this paper, a low-power LDO in combination with a switchable chip-integrated fuel cell stack was presented. The FC stack serves as energy source to power the LDO and the connected load. The feedback of the LDO and an additional fine adjustment circuit can be modified via 3 digital input signals in 6 steps. This allows an adaptation of the output voltage for different modes of operation e.g. sleep, active or data acquisition mode of a connected system. To achieve high efficiency, not only the LDO is adjusted to the output voltage needs but also the FC stack's connection is adapted. Hence, the dropout of the LDO can be kept low and the system efficiency is increased compared to an LDO with a constant input voltage. Measurements show a total current consumption of $I_{q,LDO} \leq 1.74$ µA and a maximum LDO output current of approximately 225 µA at a stabilized output voltage of 1.8 V. Due to the robust design the circuit can cope a deviation of the resistance of more than 50%. This variation in the bias network leads to decreased current consumption. In future runs the process parameters will be re-adjusted to better match the targeted resistance values as well as the output voltage and current consumption.

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