FULLY MONOLITHICALLY FABRICATED SI ONE-CHIP MINIATURE FUEL CELL

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Abstract: A novel monolithically fabricated one-chip miniature fuel cell was proposed and power generation was demonstrated. In the fuel cell, porous Si, which is formed by anodization of crystal Si in HF containing solution, is a key feature and catalyst porous Pt layer is produced with the porous Si. A through-chip porous Si layer was formed by anodization in a HF containing solution. Then, polymer electrolyte solution was immersed into the porous Si layer and the electrolyte layer was formed. Anode and cathode catalyst layers were made simultaneously on the both sides of the through-chip porous Si layer by replacing porous Si to porous Pt. A prototype cell with 110μm in thickness showed maximum output of 17mW/cm2.

Keywords: a few meaningful key words describing the essential topics of the paper, separated by commas

INTRODUCTION

Portable electronic devices have driven research toward small electric power sources. Li ion batteries are widely used and the performance of the batteries is still increasing. At this point, there are no serious complaints about Li ion battery. However, explosion of the batteries were sometimes reported. Besides, recent smart phones need frequent battery charging and the charging is not trivial matter in practical use.

Then, fuel cells have attracted large attention as ultimate portable power sources and many research groups have studied about miniaturization of fuel cells[1-8]. Recently, a miniature fuel cell system was put into market and limited number of products was sold[9]. For engineers, the fuel cell system was quite compact, however, it seemed that the cell was still large and heavy for usual consumers and the cell seemed not successful commercially. While in the recent trend of clean energy system, fuel cells are considered as one of key technologies. The portable miniature fuel cell will be attractive devices in various fields if the system would be compact enough. Therefore, we have developed miniature fuel cells with monolithically fabricated Si electrodes and reported results in the past PowerMEMS workshops[10-12].

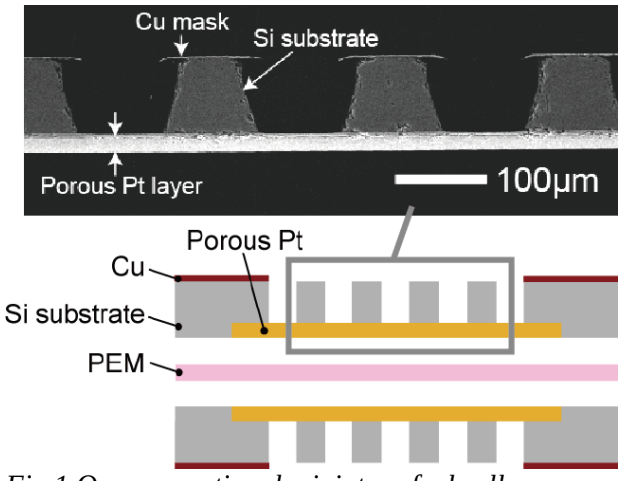


Fig.1 Our conventional miniature fuel cell.

In our miniature fuel cells, two Si electrodes were hot-pressed onto either side of a PEM (polymer electrolyte membrane) and the prototype fuel cells were built. Recently, relatively high power density of 520mW/cm^2 at 313K with H_2-O_2 supply was demonstrated and Pt usage was reduced to around 0.2mg/cm^2 as reported in the last PowerMEMS 2010[12]. The performance of the prototype cells is approaching to practical requirement. However, hot-pressing process of the three components is problematic and does not suit perfectly with MEMS batch process. Therefore, we have desired fully monolithic fuel cell structure and recent approach could achieve a preliminary prototype. In this paper, we report the novel monolithic fuel cell structure using our porous Si based technology[13].

NOVEL CELL DESIGN

In our previously reported miniature fuel cells, porous Si, which is formed by anodization of crystal Si in HF containing solution, is a key feature and catalyst porous Pt layer is produced with the porous We attempted to use this key feature and devised a novel structure.

Our Conventional Miniature Fuel Cell

The fuel cell design we proposed previously is shown in figure 1. The electrode plate has quite simple structure, in which catalyst layer and fuel channels are monolithically fabricated on a Si wafer. A highly

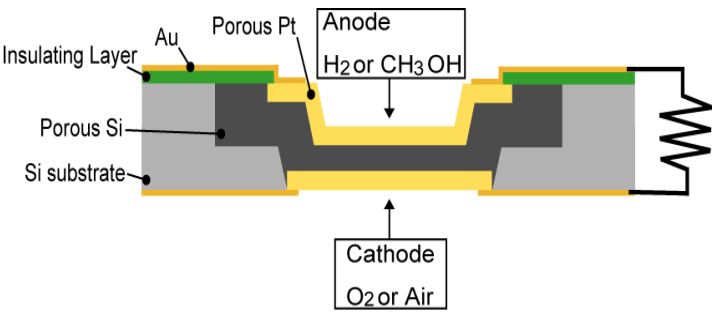


Fig2 New fully monolithic fuel cell design.

doped Si wafer, that has low resistivity, works as a current path. PEM (Polymer Electrolyte Membrane) is hot-pressed with two Si electrodes. Brief fabrication procedure for the electrode plate is written below. Cu thin film is deposited on the Si wafer by sputtering after removing oxide from the Si wafer by HF. Using usual photolithographic patterning, fuel channel Cu mask is formed for plasma etching. After the copper thin film patterning, porous Si layer is formed on the opposite side of the Si wafer by anodization in a solution containing HF. The porous Si layer is subsequently submerged into a Pt plating bath and porous Pt layer is obtained. Detailed description about porous Pt layer formation can be seen in ref.[13]. Fuel channels are opened by applying plasma etching on the backside of the porous Pt layer. In this plasma etching process, porous Pt layer works as a stopping layer of the etching and through-chip porous Pt layer is fabricated.

Though, relatively high output was obtained with some prototypes, hot-pressing is a delicate procedure and reproducibility was not good. The interface between PEM and electrodes is a problematic element not only in our miniature fuel cell but in larger scale PEM fuel cells generally. Therefore, the cell without hot-pressing was desired.

Novel Structure

Figure 2 shows our new cell design. Si is an attractive material for MEMS fabrication process and the porous Si based catalyst layer formation technique used in the above process seemed quite useful for us, and the same catalyst formation technique is employed.

On a Si wafer, through-chip porous Si layer is formed by the anodization process, and catalyst porous Pt layer is formed on both sides of the through-chip porous Si layer simultaneously by the wet immersion plating. By filling electrolyte into remaining porous Si layer in the middle of the porous layer, the through-chip porous area is expected to work as a electrolyte layer. There are a few studies about using the through-chip porous Si as electrolyte membranes[14,15] and high performance was reported by Moghaddam et al.. In those studies, catalyst layers were formed by spraying catalyst powder dispersed ink. Therefore, it is supposed that the interface between the electrolyte layers and the catalyst layers is still problematic. Proposed process makes the porous Si to porous Pt catalyst, and a new structure is expected to have continuously changing layers from catalyst to electrolyte. Then, smooth ionic conduction from catalyst to electrolyte might be achieved. It is also expected that the new monolithic structure suits MEMS batch process.

FABRICATION PROCESS

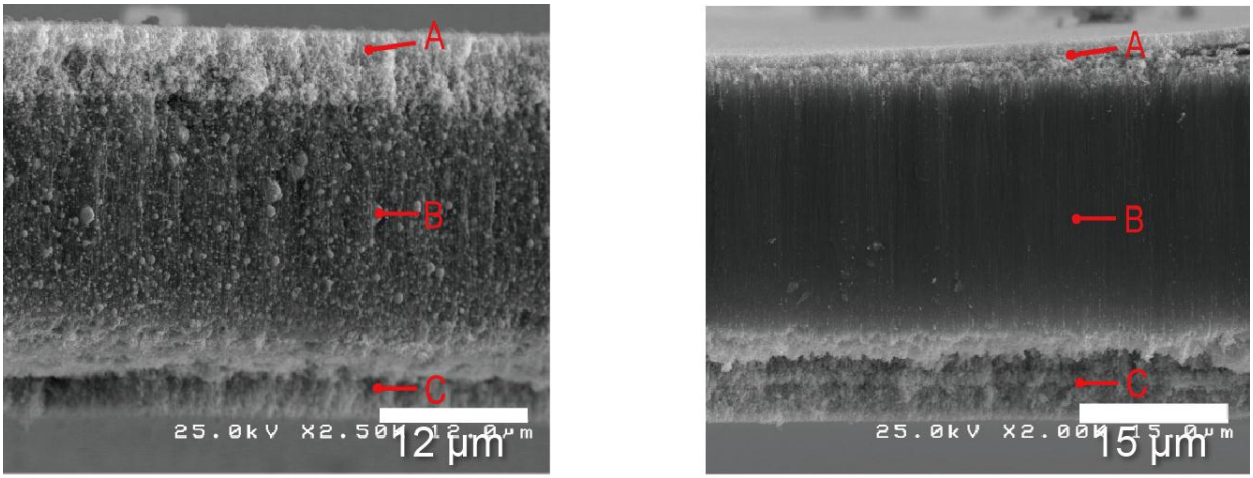
The Si wafers used in this work were n-type, 110μm thick, (100)-oriented, mirror-polished on both sides and P-doped 0.008-0.02 Ωcm resistivity. Thermally oxidized film was formed on both sides. Si wafers were cut into pieces, 15 mm square.

Through chip porous layer

Using photolithographic patterning, the oxide film was etched and rectangular openings for the through-chip porous layer were formed on the Si wafer. Concave pits were etched by TMAH solution at the openings until the remaining thickness of the substrate reduced to 50um. The oxide film on the opposite side was removed. Anodization was performed on the pit side and anodization was stopped a few um before the porous layer reached the opposite side. Then, the remaining bulk Si crystalline was removed by reactive ion etching (Samco RIE-10N). The pit side of the wafer was also slightly etched to remove small pore region formed on the top surface of anodized porous Si layer. Finally, through-chip porous layer was obtained.

Filling Electrolyte into the Porous Layer

Moghaddam et al. demonstrated very sophisticated method for the electrolyte layer formation[15]. The objective of this study was verification of the new monolithic structure, and simple process for the electrolyte layer formation was employed, though



(a) Preliminary result. *(b) After some optimization*

Fig.3 Through-chip porous layer after the Pt immersion plating.

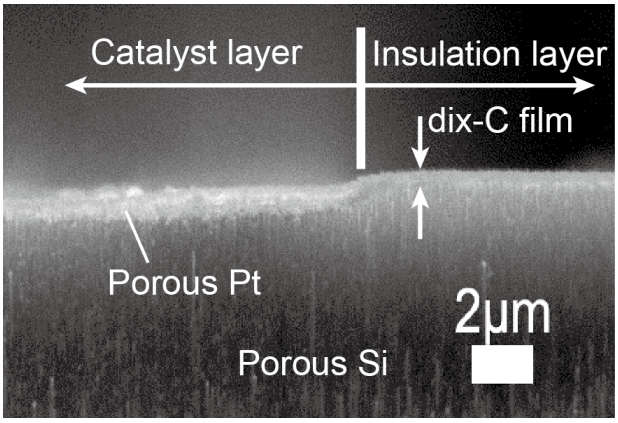


Fig.4 Edge of the polymer insulation layer.

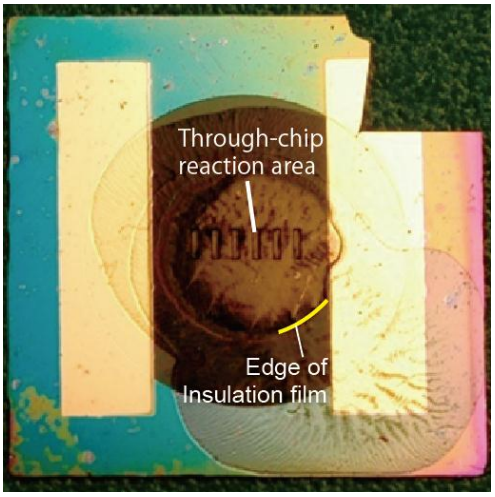


Fig.5 Top view of the prototype fuel cell.

good performance is not expected. Nafion solution diluted with IPA (isopropyl alcohol) was used as an electrolyte. The Nafion solution was put on the pit side of the wafer for specified time. Then, the residual solution was rinsed by IPA and pure water.

Insulation Between Anode and Cathode

The Si wafer used in this study is heavily doped and is almost conductive. Insulation between anode and cathode is needed. It is known that the porous Si has large resistivity and is considered as an insulator. Then, the anode or the cathode catalyst layer must be insulated from the bulk Si substrate. In this study, insulation film was coated on the substrate as shown in figure 3. CVD was performed for the film formation using dix-C (dichloroparacyclophane, similar to Parylene). The film was patterned with a hard mask during the CVD process. The film has high chemical resistance, and it is expected that porous Si is kept under the insulation film. The edge of the film partially covered the porous Si layer and contact of catalyst layer to the bulk Si crystalline is avoided.

Porous Pt Catalyst Layer

The identical way for our conventional catalyst formation using immersion plating was employed for the catalyst porous Pt layer formation. Plating bath consists of 1M sulfuric acid, 20mM [PtCl6]2- and 400mM HF. The Si wafer was immersed into the bath for 15min and 5um thick porous Pt layer was formed on both sides of the chip simultaneously. After the catalyst layer formation, collecting electrode wiring was formed by depositing Cr and Au film.

RESULT AND DISCUSSION

Prototype Fabrication

Figure 3 shows cross-sectional images of the through chip porous layers after the plating. In the preliminary results, many Pt deposits were found in the middle of the porous layer as shown in figure 3(a), that destruct insulation between anode and cathode. After some trial and error, it was found that oxide formed during the time between anodization and plating had large impact on the indesirable Pt deposits. Then, the wafer was rinsed with dilute HF solution just before the plating and desired porous Pt layers on both sides of the through-chip porous layer was obtained as shown in figure 3(b). EDS (Energy dispersive X ray spectroscopy) showed Pt contents of 83%, 2% and 92% on points a,b and c in figure 3(b), respectively, and successful catalyst layers formation was expected.

Figure 4 shows cross-sectional images around edge of the insulation film layer before the collecting electrode film deposition. It is found that catalyst Pt is not deposited under insulation film and the Pt is deposited from the edge of the insulation film. It is found that the insulation film worked as a mask for the plating process using HF, whose high reactivity we concerned about. Very smooth interface among porous Si, porous Pt and insulation film was successfully achieved.

Figure 5 shows a top view of the prototype cell. Six rectanglar trenches are the through-chip porous reaction area. Two thick gold films are the collecting electrodes and they have small contact region to the porous Pt catalyst area on the edge of the insulation film. Yellow line shows a part of the circular edge of the insulation film.

Power Generation

The prototype cell was put into an aluminum casing in a same way as our conventional miniature fuel cells. The casing has trenches for gas flow whose width and depth were 5mm and 0.1mm, respectively. Power generation test was performed in a thermostatic chamber at 318K. In order to humidify electrolyte layer, H2 fuel gas was supplied bubbling through a water bottle at 318K. The flow rates of H2 and O2 gases were 6 and 3 sccm, respectively. Figure shows a polarization curve. Peak output of 17mW/cm^2 was observed. However, observed open circuit voltage was just 473mV while conventional fuel cell shows about 1V. Besides the polarization curve was almost linear. These results suggest that serious fuel cross over happened between anode and cathode, and resistivity of current collector was high. It is obvious that the electrolyte layer formation process was preliminary

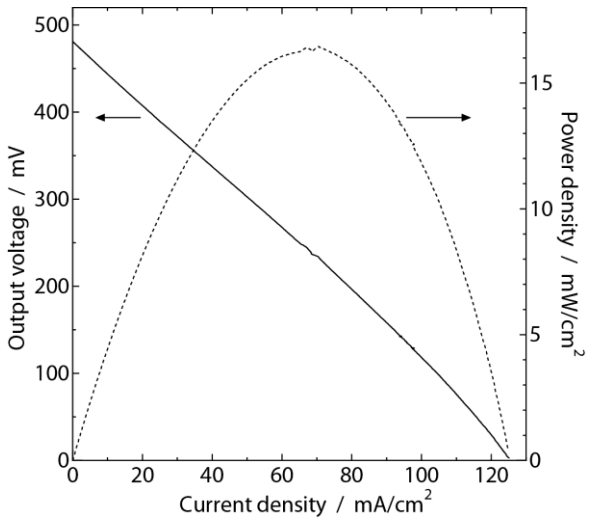


Fig.3 Polarization curve of the prototype cell.

and the performance of the layer was inadequate. Further improvement is needed especially in the electrolyte layer.

CONCLUSION

A novel one-chip miniature fuel cell was proposed. Prototype cell was built and thickness of the cell was 110um. Power generation was successfully demonstrated and peak output of 17mW/cm2 was observed. The poor output and low open circuit voltage suggest serious fuel cross over between anode and cathode. The electrolyte layer formation process was obviously preliminary and further improvement is needed. Our strategy for a novel miniature fuel cell was successfully verified and we will continue to study the structure.

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