DESIGN AND PERFORMANCE EVALUATION OF CMOS-INTEGRATED POWER PROCESSING INTERFACE FOR BENDING BEAM PIEZOELECTRIC ENERGY HARVESTERS

Nasrin Rezaei, Ahmadreza Tabesh*, Rasoul Dehghani
Department of Electrical and Computer Engineering, Isfahan University of Technology, Isfahan, IRAN
Emails: n.rezaei@ec.iut.ac.ir , a.tabesh@cc.iut.ac.ir , dehghani@cc.iut.ac.ir

Abstract: This paper presents the design of a CMOS integrated circuit for power processing of a piezoelectric energy harvester device. The designed circuitry includes an integrated circuit for the rectifier and step-down converter blocks of the power processing unit. It uses 0.18 CMOS technology to reduce the power consumption of the circuit and to improve the efficiency of the power converter. The performance of the designed integrated step-down converter was evaluated using time-domain simulation via electronic software tools. It has been shown that the efficiency of the converter for the fixed duty-cycle of 10% remains above 87.2% in a wide range of frequencies.

Keywords: CMOS integrated, energy harvester, piezoelectric bending beam, power management,

INTRODUCTION

Recent advances in low power electronics have deployed usage of wireless sensor nodes (WSNs) in a wide range of applications such as environment, medical, and structural health monitoring [1]. Batteries are the primary source of power for wireless sensor nodes. However, limited lifetime of a battery is the main challenge in usage of WSNs when they are distributed in wide area. Using an energy harvester combined with a battery has been considered as a viable solution for increasing the lifetime of the battery in a WSN. Among vibration-to-electricity energy harvesters a piezoelectric bending beam can supply micro- or milli-watt power at a suitable voltage level for electronic devices. The piezoelectric energy harvester is inherently a capacitive ac current source. Thus, to be useful for powering of an electronic device, a piezoelectric energy harvester requires an ac/dc converter that can be simply a diode rectifier.

It has been shown that a diode bridge rectifier alone is unable to efficiently capture maximum available energy of a piezoelectric beam due to mismatching between impedance of the piezoelectric beam with that of the load [2]. A solution for matching the piezoelectric impedance with the load impedance is to use a power processing unit. The power processing unit can be a dc/dc converter in series with a diode bridge rectifier [2,3].The efficiency of the conventional converters with discrete components significantly reduces at low power levels typically less than 20 mW. The main reason is the non-scalable power consumption of the converter control circuitry which becomes comparable with the output power at low power levels.

Using improved control circuitry based on ultra low power control circuitry, a power processing unit with discrete components can be used in power levels above hundreds of μW. However, in a low power range (less than a hundred μW), a discrete power processing interface is not an efficient solution since the power loss of the control circuitry outweighs its load matching advantages. Previous experiment test results of a control circuit with discrete electronic components show that the efficiency of the dc/dc converter can be reduced down to about 10% at power levels less than 100 μW which makes power converter useless [3].

The main limitations of a converter with discrete components at low power applications are two folds: power losses due to the switching phenomenon; and the gate-drive current of the internal capacitance of a switch. A potential solution is to use an integrated power processing unit instead of using power converters based on discrete components. An integrated power processing unit can be optimized based on features of a low power energy harvester. Specifically, via design of dedicated power switches, the gate-drive current can be significantly reduced. This allows using higher switching frequency at low power losses since the power consumption of gate drive circuitry can be reduced. Furthermore, using the ultra low power CMOS technologies one can significantly reduces the total power losses of the power processing converter and its control circuitry.

This paper reports on the design of an integrated power processing unit using 0.18 CMOS technology. The designed circuit includes a rectifier unit and a dc/dc power converter. The rectifier unit is designed based on voltage doubler circuit which rectifies and also increases the rectified voltage level. This CMOS technology is limited with low operating voltage which is not match with a wide range of piezoelectric output voltage up to several volts. Therefore, a circuit design technique has been used herein to develop a high voltage doubler rectifier based on low voltage CMOS technology. The paper also deals with the design of an integrated buck converter which includes a MOSFET switch with small width of PMOS which reduces the gate drive current of the circuit. The performance and efficiency of the designed circuitry has been evaluated via time-domain simulation of the electronic circuit.

STRUCTURE OF A POWER PROCESSOR

A piezoelectric bending beam energy harvester can be electrically modeled as an ac current source in parallel with an internal capacitor. The end user of this energy harvester is an electronic device that requires power with a dc voltage at a few volts. Therefore, the first stage of a power processing unit is often a diode rectifier. Figure 1 shows the block diagram of a power processing unit with a voltage double as a rectifier at the first stage. The voltage doubler increases the rectified voltage level up to about twice of the piezoelectric peak voltage. Increasing the voltage causes power transformation at lower current which in turns reduces the power losses in electronic components.

The next stage is a dc/dc converter which is mainly used for load voltage/impedance matching. The end user device is typically a battery with a voltage range from 1 to 3 volts whereas the piezoelectric open circuit voltage can be easily reach up to about several voltages. It has been analytically shown that the maximum power will be transferred only at a specific rectifier voltage level, that is, $0.5V_{oc}$ for a full bridge and V_{oc} for a voltage doubler where V_{oc} represents the piezoelectric open circuit peak voltage [2, 3]. Thus, the direct connection of the rectifier to a battery with a fixed voltage significantly reduces the efficiency of the energy harvester. The dc/dc converter can solve the matching problem by adjusting the input voltage of the converter via adjusting the duty-cycle of the switch; i.e. the output of the controller on Fig. 1. The controller adjusts the duty-cycle based on piezoelectric voltage feedback.

In micro-watt power applications, it is essential that the interface circuit dissipations remain as low as a fraction of the output power. This requires electronic circuits with ultra low quiescent power consumption less than tens of micro-watts. In addition to the circuit power consumption, the switching phenomenon of the dc/dc converter directly impacts on the efficiency of energy harvester circuitry. Using CMOS integrated circuits for power processing is a solution to reduce power dissipations of the circuit components and switching circuit losses as elaborated in the following section.

INTEGRATED POWER PROCESSING UNIT

The designed circuit herein includes an integrated voltage doubler and a switching (buck) converter as shown on Figs. 2 and 3. The open circuit peak voltage of the piezoelectric can easily pass the maximum allowable voltage of the CMOS circuitry. Thus, the designed circuit should withstand the piezoelectric high voltage levels up to several volts.

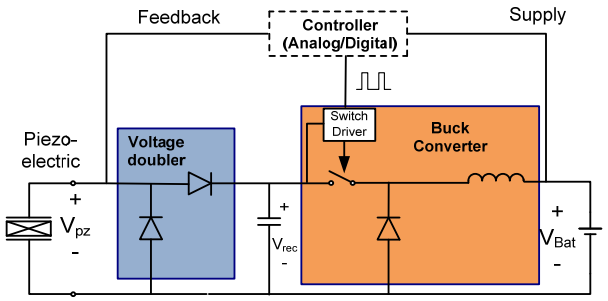

Fig. 1: Schematic diagram of energy harvester circuit

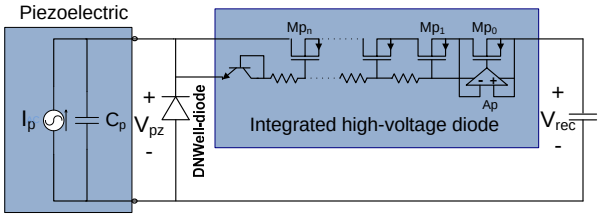

Fig. 2: High-voltage topology for voltage doubler

High-voltage integrated voltage-doubler

Figure 2 shows a circuit realization for integration of the voltage doubler block as shown in Fig. 1. The filter capacitor of the rectifier is assumed adequately large such that V_{rec} is almost constant with negligible ripples. In Fig. 2, the DNWell-diode and the active diode (combination of Mp_0 and comparator Ap) are used as the rectifier diodes for realization of the voltage doubler. A method of protection of the active diode against the high voltage of a piezoelectric is to use stacks of PMOSs with series interconnections [5], as shown in Fig. 2. This method allows operation of integrated rectifier at voltage levels up to about a few voltages.

During the negative half-cycle of the piezoelectric current source, C_P discharge and then DNWell-diode is ON. Therefore, the voltage across the harvester remains constant at $-V_D$ and no current flows toward the output during the negative half-cycle. Thus, if the voltage across each resistor is less than gate-to-drain and source-to-drain breakdown voltage limits, then Mp_n (n=0,1,2,3) will not be stressed. During the positive half-cycle, the charging current flows into the C_p. As soon as positive input (V+) of Ap becomes lower than its negative input (V-) by a small offset voltage, Mp_0 will be turned on supplying a current to V_{rec}. In this case, Mp_n will enter into the triode region and DNWell-diode will be in the reverse bias mode with a reverse voltage up to V_{rec} since in a DNWell-diode, the breakdown voltage is higher than 14 volt for the selected CMOS process [5]. Therefore, by neglecting the voltage drops on Mp_n in triode region, V_{rec} can be as high as 14V in this topology.

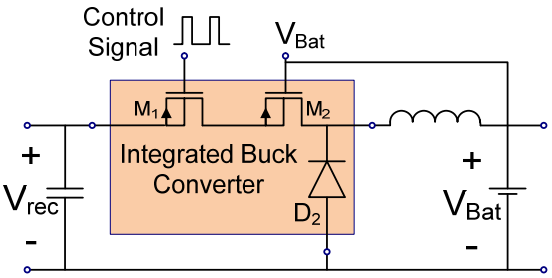

Fig. 3: Schematic of high voltage buck converter

High voltage buck converter

In the buck converter of Fig. 1, the output voltage is fixed at V_{Bat}. In this topology, the control signal adjusts the operation of the converter such that the input voltage of the converter, V_{rec}, is maintained at a pre-specified voltage level. This is a necessary condition for capturing the maximum power from piezoelectric device that regardless of variation in V_{oc}, the rectified voltage V_{rec} is adaptively adjusted at $0.5V_{oc}$ for a full-bridge rectifier and V_{oc} for a voltage doubler topology. The buck converter is used to efficiently convert the varying rectified voltage to the constant output voltage (V_{Bat}). The control strategy for adjusting the rectified voltage is based on turning on/off the switching converter with a fixed duty-cycle ratio. Turing off the converter increases the rectified voltage and turning on the converter decreases the voltage. Therefore, by comparing the rectified voltage with a reference voltage, the controller can regulate the rectified voltage at its reference value.

The rectified voltage level can easily exceed the maximum allowable voltage of the CMOS circuitry. Therefore, stacked MOSFETs are used for implementation of the buck converter switch [6]. As shown on Fig. 3, the gate of M_2 is constantly biased at V_{Bat} and the gate of M_1 is switched between V_{Bat} and V_{rec}. Thus, the voltage $V_{rec}+V_D$ is evenly distributed over both MOSFET transistors in the off-state. For implementation of the diode in buck converter, similar to rectifier section a deep N-well diode is used which can withstand high reverse voltage. The voltage drop across the pMOS resistance is:

$$V_{DS} = R_{chanel} I_{DS} \qquad (1)$$

R_{chanel} is the MOSFET resistance given by:

$$R_{chanel} = \frac{1}{\mu c_{ox} \frac{W}{L}(V_{GS} - V_{th})} \qquad (2)$$

where V_{GS}, and V_{th} are gate-source and threshold voltages, and C_{ox} and μ are gate oxide capacitance per area and electron mobility, respectively. W and L represent the width and length of MOSFET channel, respectively. Based on (2), the larger the W/L ratio is, the smaller the conducting loss will be. However, gate-drive current is also directly proportional to both W and L. In low power applications the gate-drive losses due to gate capacitive current dominantly impacts on the efficiency of the converter [2]. The output current of a cm-scale piezoelectric energy harvester is in the range of μA. Thus, the conduction loss of the switch is relatively small compared to switching losses of the converter. Hence, the W/L ratio of the transistors is chosen small to reduce gate-drive losses. The discrete MOSFET transistors for switching power supply applications are mainly designed for power rates well above a few watts. This requires a relatively large W/L compared to that of required for a milli-watt scale transistor for energy harvesters. The significant advantage of using integrated power processing unit is the capability to design dedicated MOSFET with minimum W/L ratio, optimized for energy harvesting applications.

CIRUIT PERFORMANCE EVALUATION

The preliminary work presented herein is focused on the design of an integrated low power voltage-doubler and buck converter which can withstand high voltage levels of piezoelectric device. To evaluate the performance of the designed circuit, a study system is modeled and the circuits operations are evaluated using this system. The piezoelectric beam is assumed to be a cm-scale bending beam energy harvester. The dimensions of a sample two-layer beam with parallel connection are: 31.7mm length, 12.7mm width, 0.51mm thickness. The internal capacitance and resonance frequency of the beam with PZT5A material are calculated as C_p=26.5nF and ω_n=483.5Hz, respectively. The end-user of this energy harvester is a 2.57V rechargeable battery as shown in Fig.1. The voltage-doubler and buck converters are designed based on detailed schematics on Fig. 2 and Fig. 3 using 0.18um CMOS technology.

The circuit simulation results are shown on Fig. 5 to Fig. 7. The normalized rectified voltage with respect to the piezoelectric open circuit voltage is depicted on Fig. 5 for Voc from 3 to 6 volts. Theoretically, the Vrec/Voc ratio must be constant at 2 for a range of Voc. However, as the figure shows, this ratio starts from 1.55 at Voc=3V and increases to 1.75 at Voc=6V. This is because of the voltage drop across the voltage doulber diode and stacks of PMOSs as well as current consumption of the comparator. As the open circuit voltage increases the contribution of the voltage across the diode and PMOSs will become less, thus, the circuit becomes more efficient. Figure 6 (a) shows the measured efficiency of the buck converter for the fixed duty-cycle ratio 10% at a wide range of frequency from 100 Hz up to 5kHz. As the graph shows, the efficiency is ranged from 88.2% at low frequencies down to 87.2% at high frequencies.

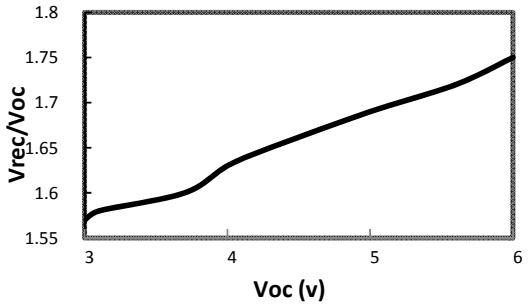

Fig. 5: The normalized rectified voltage (Vrec/Voc) versus Voc.

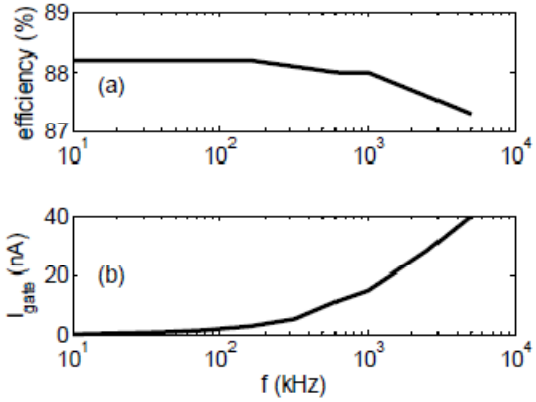

Fig. 6: (a) The efficiency of the power converter versus switching frequency; (b) The gate current versus frequency at duty-cycle D=10%.

Previous experimental results of a buck converter with discrete components show maximum efficiency of 60% at power level less than 10mW [3]. Therefore, the designed integrated buck converter is more efficient compared to a converter with discrete components.

The graph on Fig. 6 (b) shows that the gate current of the buck converter switch increases as the switching frequency increases at a fixed duty-ratio. However, since the MOSFET switch in the integrated converter is designed with a small W/L ratio, this gate current is small compared to circuit with discrete components which results a converter with higher efficiency at low power applications. Figure 7 shows the efficiency of the power converter with respect to the input power which is above 85% for input power up to 250 µW. Compared to converters with discrete component with maximum efficiency of 60% for this range of input power, the design integrated circuit is more efficient.

CONCLUSION

The preliminary design of a CMOS integrated circuit for power processing unit of a piezoelectric energy harvester device is presented. The proposed circuit adopts high-voltage design techniques using a conventional CMOS technology to design the rectifier and step-down converter blocks of the power processing unit.

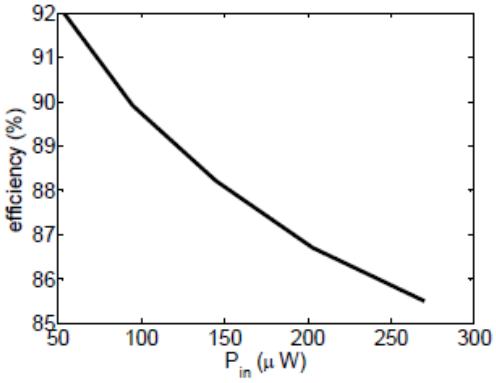

Fig. 7: The efficiency of the power converter versus the input power.

It has been shown that integration of the power processing unit can significantly improve the efficiency of the unit compared to the power processing units with discrete components. A comparison of measured efficiency for a sample circuit with discrete and simulation results of the integrated circuit variant show that integration of the power processing unit at power levels less than 250 µW can be improved at least 30%. Improving the efficiency at low input is important in the design of self-power portable electronics based on energy harvesting as a source of energy.

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