

# MICROWATT ELECTRONICS AND BEYOND

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**Abstract:** Advances in process technology and circuit design are enabling new applications for low power electronics. Increasingly, complete systems performing communication, sensing and processing functions can operate from microwatt power levels, well-suited for powering by energy harvesters. In this paper we review recent advances in low power systems, touching upon trends and techniques that allow microwatt operation and beyond. Challenges of operating from a harvested energy source, and considerations for the interface and energy processing circuits, are also discussed.

**Keywords:** low power electronics, low voltage, body area networks, sensor nodes, energy harvesting

## INTRODUCTION

Advances in process technology and circuit design are enabling new applications for low power electronics. Increasingly, complete systems performing communication, sensing and processing functions can operate from microwatt power levels, well-suited for powering by energy harvesters. Much recent research has been driven by two application areas which will be the focus of this discussion: biomedical monitoring devices and autonomous sensors. In the former, small nodes are used to acquire and process physiological signals such as body temperature, movement, or electrical signals from the heart (ECG), muscles (EMG) or brain (EEG). These devices may be used during sports, or for continuous monitoring of subjects' vital signs either in homes or hospitals. In these cases, small form factors, low energy consumption and long operating lifetimes are essential. Similarly, autonomous sensors [1] may be used for surveillance, to monitor buildings, or deployed in the environment for scientific studies. When the sensors are deployed over a large area, long battery lifetimes or the ability to operate from harvested energy is even more important.

Low power systems generally require the basic electronic building blocks sketched in Fig. 1: an analog front-end to the sensors, processors to control the overall system and to analyze the acquired signals, communication either through wireless or wireline, and finally a power management block that powers all the components. The following sections will discuss what is achievable at different power levels for each of these components, and give examples of state-of-the-art systems.

## FRONT-END SIGNAL ACQUISITION

The front-end circuitry serves as interface to the analog world, for example to accelerometers, temperature sensors, EEG electrodes, etc. In order to

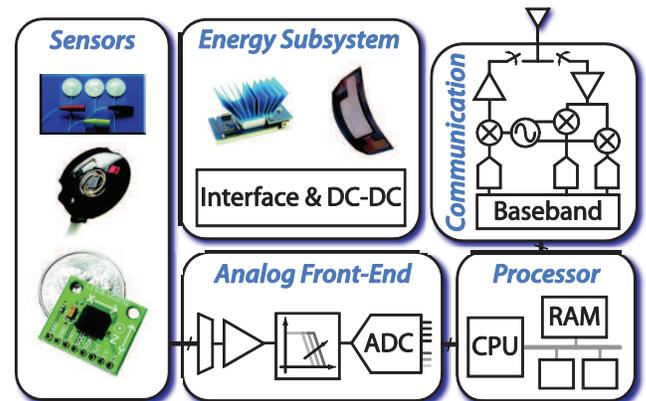


Fig. 1: A typical low power processing platform.

achieve good performance and low power, front-end circuits are often highly customized for the application. For example, a typical analog front-end for biomedical monitoring devices contains an instrumentation amplifier, anti-aliasing filter, and analog-to-digital converter (ADC) as seen in Fig. 1. In this context, the front-end needs to amplify signals ranging from  $\mu\text{V}$  to  $\text{mV}$ , while rejecting power line interference, electrode offsets, and device noise. Nevertheless, recent research has demonstrated many efficient front-ends. Instrumentation amplifiers for  $\mu\text{V}$  EEG signals, with bandwidths up to  $\sim 100\text{Hz}$  and input-referred noise of several  $\mu\text{V}_{\text{rms}}$ , consume on the order of several  $\mu\text{W}$  or even hundreds of  $\text{nW}$  [2]. Techniques to achieve low power with low noise include the use of chopper architectures to suppress low-frequency noise [3][4], and system-level feedback to reduce interference at the input and relax dynamic range requirements in the remaining circuits [2].

Similarly, ADCs have undergone continuous improvements, and thus state-of-the-art designs are highly energy efficient. Fig. 2 plots the energy per Nyquist sample versus effective number of bits (a measure of resolution) for recently published ADCs

[5]. It is seen that many ADCs consume around tens of pJ per sample. Of the various ADC architectures, the successive approximation ADC (SAR) is well-suited for the moderate resolution ( $\sim 8$ -bit) and MHz sample rates that are of interest to low power systems.

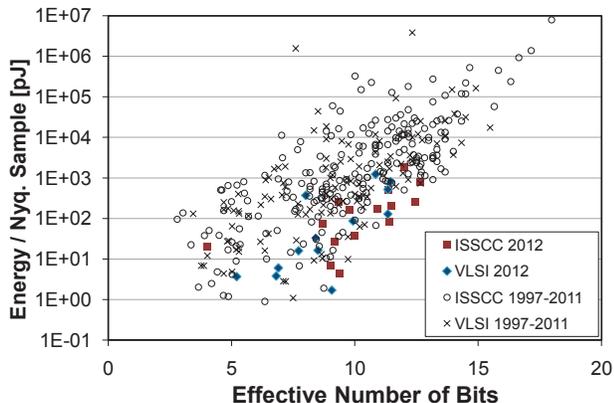


Fig. 2: Energy per Nyquist sample vs. resolution of ADCs [5].

## DIGITAL PROCESSING

The digital processing for low power systems has benefited from process scaling and low power design techniques. A full-featured ARM Cortex-M3 32-bit microcontroller can consume tens of mW at 50MHz in active mode [6], exercising a large set of peripherals as shown in Table 1. However, the processor can also be scaled down in various ways to reduce power. As a contrast, a research prototype [7] also employs the Cortex-M3 core, but has a different feature set targeted towards EEG processing (Table 1). This second processor consumes only  $0.99\mu\text{W}$  while executing an algorithm for epileptic seizure detection [7] that involves a 256-point FFT, 4-point median calculation, 128-point median filter, and an IIR filter every 0.5 seconds.

Such low power consumption is achieved by aggressively reducing all contributors, namely switched capacitance, voltage and frequency. Custom accelerators (e.g. for FFT) can be employed to perform specialized functions faster and more power-efficiently than the general-purpose CPU, resulting in order-of-magnitude improvement. Blocks are clock- and power-gated when they are not in use in order to further reduce switched capacitance. At the same time, voltage and frequency can be scaled down until the algorithm can barely be performed within the available time. For the seizure detection algorithm, the voltage and frequency are set to 0.8V and 16kHz respectively. For simpler algorithms, these can be reduced further to 0.5V and 7kHz, at which the

processor core and SRAM together consume 238nW.

Table 1: A general-purpose and an ultra-low-power ARM Cortex-M3 with different feature sets and frequency/power characteristics.

	Cortex-M3 [6]	Cortex-M3 [7]
Power supply	3.3V	0.5V - 1.0V
Max. freq.	50MHz	7kHz - 5MHz
Peripherals	Digital: Flash, DMA, GPIO, watchdog, timers, SSI, UART, CAN, Ethernet, PWM, quadrature encoder interface Analog: LDO, comparator, ADC, temp. sensor	Digital: DMA, GPIO, timers, SPI, FFT, ADC interface

In the range between mW and nW, many micro-power processors have been demonstrated. For example, a 1024-pt FFT processor consumes 600nW at 0.35V [8], and an 8-bit processor consumes 2.6pJ per instruction at 0.36V, 833kHz [9]. These processors utilize a power supply near or below the transistor threshold voltage, since the energy per operation (or energy per clock cycle) of the processor is typically minimized in this region [8] as shown in Fig. 3. At a nominal supply voltage ( $\sim 1\text{V}$ ), the energy per operation is dominated by active  $CV_{DD}^2$  energy, so as  $V_{DD}$  scales down, the energy per operation decreases quadratically. However, at low supply voltages ( $< 0.4\text{V}$ ), the energy per operation is dominated by leakage energy since leakage power is integrated over a long clock period. These opposing trends produce a minimum in the energy per operation curve which often occurs around the transistor threshold. Accordingly, micro-power processors function near this point if the clock frequency can be relaxed. If the application involves bursts of high speed activity in between long periods of slow tasks, the processor can dynamically elevate the supply voltage during the high activity periods, but handle background tasks at the energy-optimal point [10].

Due to the sheer number of transistors involved, digital blocks (including memory) often contribute a large portion of the leakage power in a system. For energy harvesting applications with low duty cycles, managing leakage is essential. A common approach is to disconnect circuits from the power supply via power switches (i.e. power-gating), but the processor state is lost and needs to be restored after wake-up. An emerging technology is the use of low power non-volatile memory such as ferroelectric memory [11] as the main random access memories in such systems.

Aggressive techniques can further suppress the leakage power down to the order of pW – the Phoenix processor [12] demonstrated the use of ultra-low leakage memory and data compression in order to reduce leakage down to 30 pW.

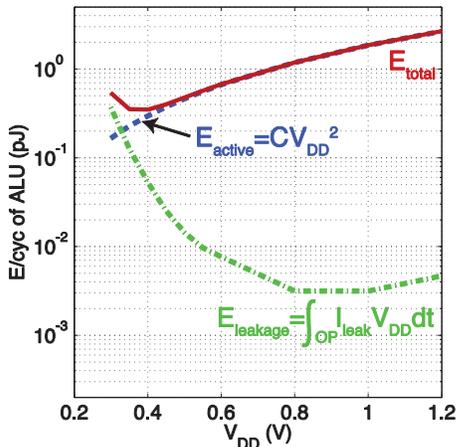


Fig. 3. Energy/cycle vs. supply voltage; the energy/cycle can be minimized by aggressive voltage scaling.

## COMMUNICATION

Low power systems often include some means of communication, both to receive configuration commands or to communicate results of the signal acquisition and analysis. Power constraints will naturally limit the range or data rates achievable, but useful communication links can still be realized.

Commercial standards have been developed for low power wireless communication. Recent works include Bluetooth Low Energy (LE) and the 802.15.6 Body Area Network (BAN) standards. In the former, the strategy to reduce average power is to allow low duty cycles, so that even though the radio peak power is typically tens of mW, the average power drops to the  $\mu$ W range with duty cycles less than 1%. At such power levels, Bluetooth LE transceivers typically have a range of tens of meters and data rates of several hundred kbps to 1-2Mbps.

On the other hand, the 802.15.6 standard specifies a narrowband physical layer designed to reduce peak power requirements. This is done by simplifying the modulation scheme to enable lower power circuits in the transceiver. In this case, the range is intended to be several meters, with data rates up to 1Mbps. As recently shown in [13], both these standards can be supported with a peak transmit and receive power of  $\sim 5$ mW, and energy/transmitted bit of 5nJ.

Transceivers in the literature targeting similar applications have demonstrated techniques to enable sub-nJ per bit energy consumption. In [14] a

transmitter for BAN employs multiple Film Bulk Acoustic Wave Resonators (FBAR) to realize low-power oscillators. Along with digitally-oriented architectures that are more amenable to voltage scaling, this results in 440pJ/bit or 440 $\mu$ W at 1Mbps. On the receive side, FBARs are used to realize high Q filters [15], relaxing the need for precise, power-hungry local oscillators. The receiver energy is reduced to 180pJ/bit, or 180 $\mu$ W at 1Mbps.

In some situations it is feasible to use wired instead of wireless links between nodes, facilitating higher data rates and energy efficiency. For instance, sensor nodes placed on the body can communicate through conductive yarn sewn into clothing (Fig. 4), reaching rates of 10Mbps at 3.2pJ/bit over a range of 1m [16]. Another interesting approach involves body channel communication, where the signal is coupled onto the body and travels along the skin to the receiver. An example transceiver [17] has demonstrated good energy efficiency, consuming 0.37nJ/bit with data rates up to 10Mbps over 1.8m.

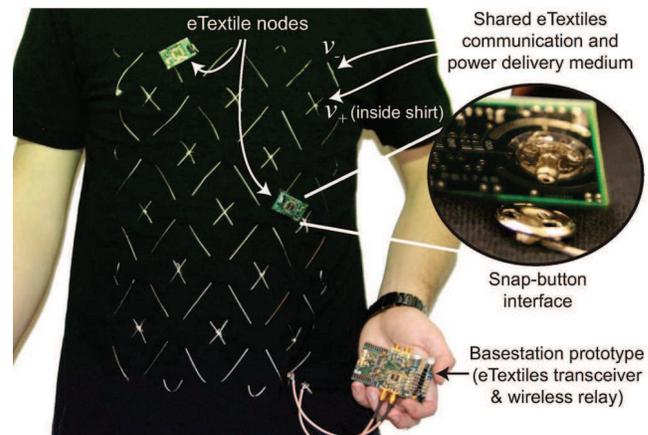


Fig. 4: Body area network nodes communicating via conductive yarn. ©2011 IEEE. Reprinted, with permission from [16].

## ENERGY PROCESSING

The energy processing block provides an interface to energy harvesters and delivers the power and voltage levels needed by the load circuits. The interface circuits face some interesting challenges. First, they must present a suitable impedance to the harvester in order to maximize power transfer. For some harvesters (e.g. solar cells), the optimal impedance varies significantly under different conditions, so maximum power point tracking (MPPT) is necessary. In addition, if the harvester output voltage is low (e.g. tens of mV from a small temperature gradient across a thermoelectric harvester), special mechanisms are needed to startup the interface circuits. Examples include use of a transformer [18] or mechanical

switch [19] to help transfer sufficient charge to a capacitor to power the rest of the interface circuits.

Since the energy provided by a harvester fluctuates depending on environmental conditions, it is desirable to use multiple types of harvesters in a system. An interface architecture for piezoelectric, thermoelectric, and solar energy harvesters [20] is pictured in Fig. 5. In order to combine energy from all these sources, parallel power converters are implemented and provide the optimal impedance for maximum power transfer from each harvester. Even so, with intelligent time multiplexing, these converters can share a single inductor through a configurable switch matrix with minimal power overhead.

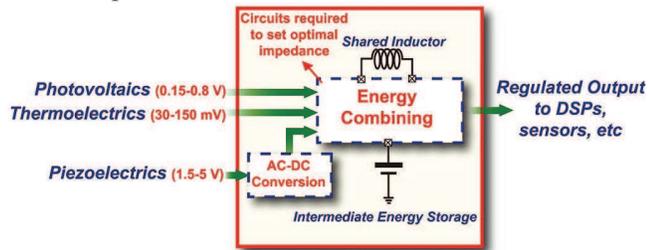


Fig. 5: A multi-input energy-harvesting system using a single shared inductor. ©2012 IEEE. Reprinted, with permission from [20].

Once energy is extracted from harvesters, the next challenge is to deliver it efficiently or store it in a battery for later use. A charger in [21] interfaces to solar and thermoelectric sources, but must also provide battery management features to detect over- or under-voltage. Further, it employs various gating techniques to lower the quiescent current to 330nA. Similarly, voltage regulators for low power systems should achieve good efficiency while delivering various low voltage and power levels required by the load circuits. An emerging approach is switched capacitor converters that can be fully integrated on-chip in micro-power systems. One such converter [22] can provide variable output voltages (0.3V–1.1V) at >70% efficiency while supplying between 5 $\mu$ W to 1mW. To do so, it employs different configurations of charge transfer capacitors to minimize conduction losses while providing variable voltages.

## PUTTING IT ALL TOGETHER

With the above components and design techniques, it is feasible to realize complete low power systems operating from harvested energy. Some recent examples also serve to illustrate system-level considerations of operating from a potentially unreliable energy source. A body area sensor node [23] is powered by a thermoelectric generator and integrates a boost converter, voltage regulator, analog

front-end (AFE), a digital signal processor, and a radio. The system functionality and power consumption scale based on the amount of available energy. With sufficient energy, all blocks are active. At lower energy levels, the RF transmitter is duty cycled, and finally at very low energy levels, power and clocks to the AFE and DSP blocks are shut off. Importantly, doing additional digital processing can help save overall system power. When the system acquires and sends a raw ECG waveform, the radio operates continuously and the system consumes 397  $\mu$ W. However, in another mode the system wakes up periodically, uses the DSP to extract heart rate and detect abnormalities, then transmits only the results. This significantly decreases the radio on-time, reducing the average system power to 19 $\mu$ W.

An intraocular pressure monitor in [24] is restricted to a cubic mm in volume due to its implantable nature, thus constraining the energy sources to a 1 $\mu$ Ah thin-film lithium battery and 0.07mm<sup>2</sup> solar cell. Accordingly, the system maintains very low average power through ultra low voltage operation (a 0.4V microcontroller consuming 90nW of active power) and powering off components during long standby periods. However, data must still be retained through an ultra low leakage SRAM. The overall average power while taking pressure measurements every 15 minutes is only 5.3nW. Since the solar cell provides >80nW on a sunny day, this system can achieve energy-autonomous operation.

## CONCLUSION

Advances in low power electronics make it possible to perform a variety of functions with only microwatts of power, including amplifying microvolt signals, sophisticated signal processing, and communication at Mbps rates. Although such circuits are constrained to operate at moderate speeds, this is sufficient for many mobile or sensing-oriented applications. Proof-of-concept systems show great promise, but also illustrate the need for architectures that scale gracefully and retain key states when available energy levels fluctuate. With continued progress on harvesters and energy-aware design, energy harvesting systems can find new exciting applications.

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