

# MINIATURE PLANAR HIGH SPEED ULTRACAPACITOR UTILIZING INTERDIGITATED CARBON NANOTUBE ELECTRODES

M.E. D'Asaro, D.P. Jenicek, and J.E. Schindall

EECS, Massachusetts Institute of Technology, Cambridge, MA, USA

**Abstract:** This paper reports the design, MEMS-based fabrication, and testing of miniature ultracapacitor electrodes grown directly on silicon using low pressure chemical vapor deposition (LPCVD) of carbon nanotubes. The capacitors use electrodes comprised of tall and narrow fingers arranged in an interdigitated pattern that allows for ease of fabrication. A high capacitance density of  $52 \mu\text{F}/\text{mm}^2$  was achieved, and also higher speed than a traditional ultracapacitor.

**Keywords:** MEMS, Ultracapacitor, Carbon Nanotubes, Integrated Energy Storage, Integrated Capacitors

## INTRODUCTION

Since the invention of the transistor in the middle of the last century, tremendous progress has been made in miniaturizing and integrating active electronic components for digital, analog, and power applications. However, much less progress has been made in miniaturizing and integrating energy storage components - high-value inductors and capacitors - and these components often take up a majority of volume in modern electronics.

In response, this work applies the technology developed by Dr. R. Signorelli and Professor J. Schindall at MIT [1] in which forests of vertically aligned carbon nanotubes are used as electrode material to create miniature ultracapacitors directly on silicon. This is not the first time that miniature carbon-nanotube ultracapacitors have been investigated - Y. Q. Jiang [2] demonstrated ultracapacitors utilizing the same interdigitated structure as in this work, but with much smaller capacitance densities and lower speeds, while H. J. In [3] demonstrated a device using an entirely different opposing electrode structure.

## THEORY

As shown in Fig. 1, an ultracapacitor consists of two porous electrodes, traditionally made of activated carbon, immersed in an electrolyte and separated by a piece of ion-permeable but electrically insulating material. When a potential is applied between the electrodes, the ions in the electrolyte migrate into the electrode with the opposite charge. These ions cancel out the fields created by the electric charges on the electrodes, allowing additional electric charge to build up, which in turn attracts more ions. This process continues until all the surface area of the electrodes is covered with ions.

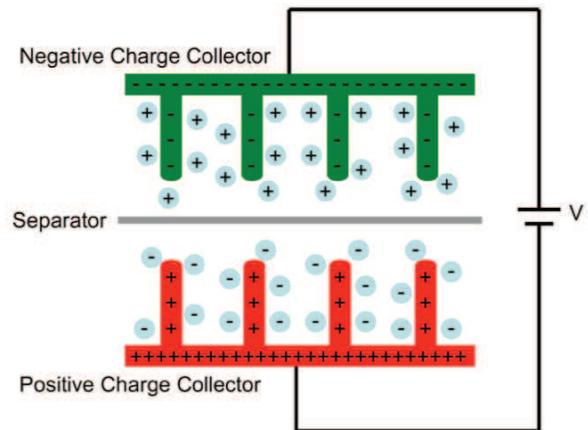


Fig. 1: Schematic of a traditional ultracapacitor.

The speed at which this process can occur, and therefore the speed at which the capacitor can be charged or discharged, is primarily limited by collisions between the ions and the electrode material as the ions migrate into and out of the electrodes [4]. This resistance that the electrode material presents to ion flow is known as ionic resistance and it can be roughly modeled, by analogy to an electronic resistance, through Eq. (1), where  $R_{\text{ionic}}$  is the total ionic resistance of the electrode,  $\rho_{\text{ionic}}$  is the ionic resistivity of the electrode material,  $L$  is the distance into the electrode that the ions must migrate, and  $A$  is the macroscopic area of the electrode material.

$$R_{\text{ionic}} = \rho_{\text{ionic}} \frac{L}{A} \quad (1)$$

Based on Eq. (1) the ionic resistance can be reduced by decreasing  $\rho_{\text{ionic}}$  or  $L$  or by increasing  $A$ . However,  $\rho_{\text{ionic}}$  is a material property of the chosen electrode material and thus is not easily modified. Furthermore, increasing the macroscopic electrode area,  $A$ , also increases the capacitance by the same

factor, and thus has no effect on the RC time constant (speed) of the device. Decreasing  $L$  will decrease the time constant of the device, but in a traditional device such as shown in Fig. 1, this comes at the expense of decreasing the capacitance of the device by the same factor.

The innovation in this work, therefore, is to use an alternative device structure, shown in Fig. 2, to get around this limitation and allow for large capacitances with low time constants. The structure consists of interdigitated fingers of electrode material grown vertically out of a silicon substrate. In this topology the ions migrate between adjacent fingers parallel to the silicon substrate. This has the advantage of setting  $L$  equal to the finger width, which, using lithographic techniques, can be made extremely small. At the same time, by increasing the number of fingers present, the total device capacitance is maintained.

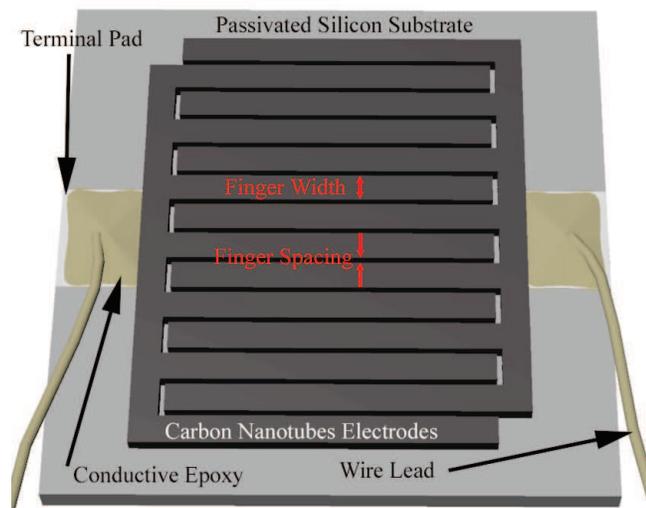


Fig. 2: Interdigitated Device Structure.

## DEVICE CONSTRUCTION AND TESTING

Device fabrication begins with a thermally oxidized silicon wafer that simulates a passivated integrated circuit. First, OCG 934 photoresist is spun onto this wafer, exposed, and developed to prepare the wafer for lift-off. Second, an AJA 3-target sputtering machine is used to deposit three layers: molybdenum (100 nm), alumina (10 nm), and iron (1 nm). The molybdenum layer is the current collector, connecting the electrodes to the outside world, the iron is the catalyst for nanotube growth, and the alumina prevents the iron from commingling with the current collector. After sputtering, the remaining photoresist is removed with Microstrip® in an ultrasonic cleaner. To complete the preparation for nanotube growth, the wafer is cleaved into individual samples. The resulting partial cross-section is shown in Fig. 3.

This structure is then placed in a custom-built LPCVD chamber, shown in Fig. 4, where 100  $\mu\text{m}$  tall carbon nanotubes grow only onto the metalized portion of the wafer in a process perfected for capacitor applications by Signorelli [1].

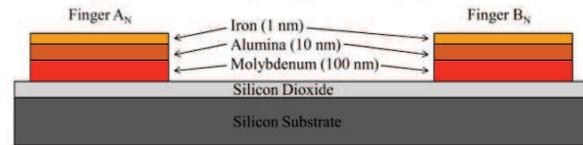


Fig. 3: Cross Section of wafer after deposition and lift-off.

The actual growth process consists of two steps: reduction and growth. In the first, reduction, the sample is held at approximately 100  $^{\circ}\text{C}$  and exposed to 642 sccm of argon and 88 sccm of hydrogen. This serves to reduce any iron oxide, which may have formed on the top of the sample, back to iron. Growth consists of heating the sample to approximately 780  $^{\circ}\text{C}$  and exposing it to a flow of 642 sccm of argon, 66 sccm of hydrogen, and 28 sccm of acetylene. Carbon nanotube growth is believed to occur when the iron layer (in the form of nanoparticles) absorbs sufficient carbon from the acetylene gas to become supersaturated, at which point the nanoparticles excrete the excess carbon, which, due to the nanoparticles' size, forms multi-wall carbon nanotubes of approximately 5-10 nm in diameter.

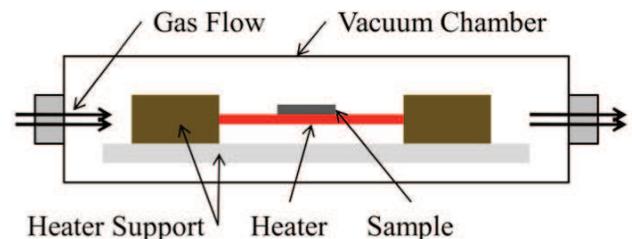


Fig. 4: Diagram of the Low Pressure Chemical Vapor Growth Deposition Chamber used to grow carbon nanotubes.

After the growth process is complete, wires are attached to the samples using silver epoxy. Because carbon nanotubes are hydrophobic, in order to wet them with the electrolyte they are first wetted with isopropyl alcohol and then rinsed with water before being submerged in a 1 M solution of sodium sulfate, an electrolyte chosen for its ease of handling and non-corrosive properties.

However, because sodium sulfate is an aqueous (water based) electrolyte, device operation is limited to  $\pm 1$  V to avoid dissociation of water by electrolysis. Testing was attempted with non-aqueous

electrolytes, such as propylene carbonate and acetonitrile, which allow operation up to 3 V but caused shorting between adjacent fingers for unknown reasons, forcing a return to sodium sulfate. Furthermore, due to the hydrophobic nature of the carbon nanotubes, wetting in sodium sulfate causes delamination of the nanotubes from the substrate after several hours, rendering the device inoperative. These challenges hindered the efficient collection of data and must be overcome to produce a practical device.

### DEVICE TESTING METHODS

To measure the capacitance of the resulting devices, a cyclic voltammeter was employed. Made by Arbin, this instrument measures the current through the capacitor while sweeping the voltage linearly between bounds of -1 V and 1 V in a triangle-wave pattern. The current is then plotted as a function of voltage, to form a plot called a cyclic voltammogram (CV). Because the current through an ideal capacitor is the capacitance times the rate of change of the voltage across it, the voltammogram for an ideal capacitor should be a rectangle with the capacitance equal to the current divided by the voltage sweep rate. Thus, the capacitance for a device is determined by dividing the current recorded on the voltammogram at zero volts by the sweep rate. The current around zero voltage is used because the apparent capacitance increases with applied voltage due to parasitic effects.

Measuring the ionic resistance of the devices was more involved because the total series resistance of the devices was much larger than their ionic resistance due to parasitic electrical resistances between the nanotubes and the current collector and in the current collector itself. To separate these effects, impedance spectroscopy was employed. In this technique, the complex impedance of the device is measured over a range of frequencies (0.1 Hz to 100 kHz in this case) and this data is then plotted with the real component on the x-axis, the negative of the imaginary component on the y-axis, and the frequency as a parametric variable. By looking at the shape of the resulting plot, the individual impedances can be separated [1]. An example of a circuit and its corresponding impedance spectrogram is shown in Fig. 5 and Fig. 6. Note that the ionic resistance is represented by a 45° line and its value can be determined by noting the length of this line projected onto the x-axis, represented by  $R_L - R_{TOT}$  in Fig. 6.

In a real impedance spectrogram the transitions between segments are less clearly defined, and due to the limited range of frequencies available, only a

segment of the entire plot is available. That said, as shown in Fig. 7, the value of the ionic resistance can still be obtained with a reasonable degree of certainty.

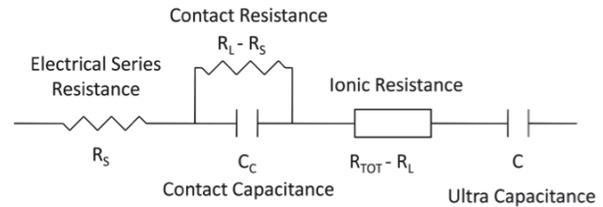


Fig. 5: Equivalent Circuit for a real ultracapacitor.

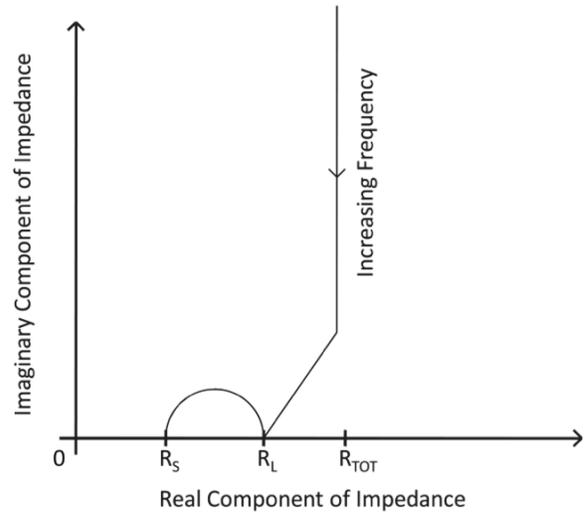


Fig. 6: Idealized impedance spectrogram corresponding to the circuit in Fig. 5.

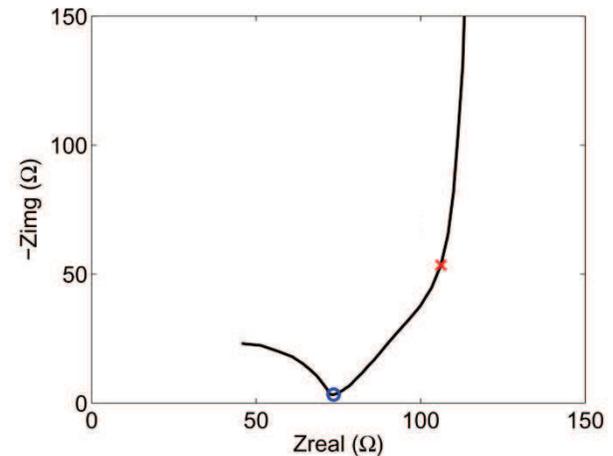


Fig. 7: Real Impedance Spectrogram for a 40  $\mu\text{m}$  finger width device with ionic resistance marked.

### RESULTS AND ANALYSIS

Two classes of devices were created. The first class used very wide fingers (500  $\mu\text{m}$ ) to maximize the capacitance per unit area and minimize the leakage, while the second class used increasingly narrow finger

widths to explore the effect of finger width on the device time constant. For the three high-capacitance devices tested, capacitance values of 0.67 mF, 1.6 mF, and 3.5 mF were obtained. The active area of the interdigitated nanotube structure, without the connecting terminals, has dimensions of 7 mm x 9.5 mm, which corresponds to 66.5 mm<sup>2</sup>, yielding a maximum capacitance density of 52.6  $\mu\text{F}/\text{mm}^2$ , which is over an order of magnitude higher than the 4.28  $\mu\text{F}/\text{mm}^2$  achieved by Y. Q. Jiang with a structurally similar planar ultracapacitor [2]. For comparison, this is over two orders of magnitude higher than for typical trench capacitors, which at about 450 nF/mm<sup>2</sup>, are the current state-of-the-art for high-value on-die capacitors [5].

Two sets of four variable-finger-width devices were created, each with finger widths of 10  $\mu\text{m}$ , 20  $\mu\text{m}$ , 40  $\mu\text{m}$ , and 80  $\mu\text{m}$ . The capacitance and ionic resistance of each of these devices was measured and the ionic resistance and the ionic-resistance - capacitance time constants are plotted in Fig. 8 and Fig. 9 respectively. Note that in both cases, the data, as predicted, indicates a roughly linear relationship between finger width and ionic resistance or time constant. The time constant plot is more linear than the ionic resistance because in finding the time constant, differences in total electrode area between samples are canceled out. The last point on the graph does not follow the trend, but this is expected given that for the 80  $\mu\text{m}$  devices, the nanotube fingers are as wide as they are tall, meaning that the assumption that ions only flow into the sides of the fingers (not the tops) is no longer true.

Finally, extrapolating from the linear fit of the time constant data to a time constant of 1.3 ms, which is the absolute minimum for any 120 Hz filtering to occur, the finger width would have to be about 1.7  $\mu\text{m}$ , well within the realm of modern lithography.

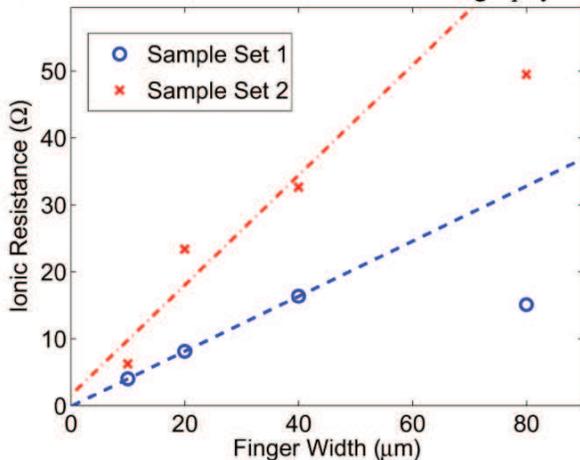


Fig. 8: Ionic resistance versus finger width.

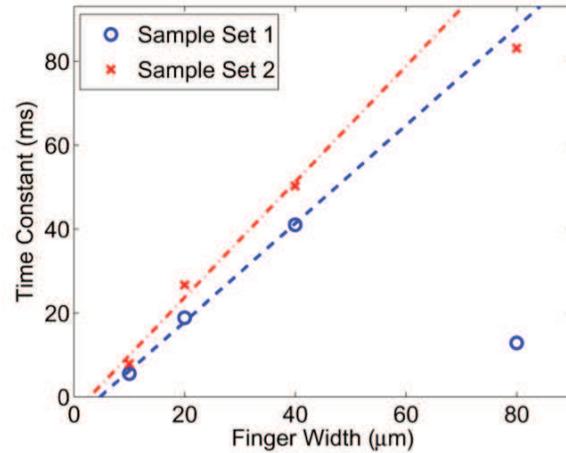


Fig. 9: Ionic-Resistance – capacitance time constant versus finger width.

## CONCLUSION

This work demonstrates that through lithographic shaping of the electrodes of an ultracapacitor, the time constant can be reduced while maintaining a high capacitance. Furthermore, a planar ultracapacitor on silicon was constructed with a higher specific capacitance than in any known previous work. These devices, when further refined, could see use in applications ranging from extremely low power devices like energy harvesters and smart RFIDs to high power applications such as a monolithic off-line power converter or LED driver.

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