

FABRICATION, MODELING AND PERFORMANCE ANALYSIS OF SILICON-EMBEDDED 3-D TOROIDAL INDUCTORS

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Abstract: This paper presents the fabrication, modeling, characterization and analysis of silicon-embedded, air-core, three-dimensional toroidal inductors for power converter applications. The inductors are fabricated within deep silicon recesses by means of a 3-D silicon shadow mask coupled with electroplating techniques. The losses in the inductor and the surrounding silicon are analytically modeled using simplified circuit models as well as energy methods, and the effects of using silicon wafers with both standard and high resistivities as embedding substrates are discussed and experimentally characterized. Inductors with inductances of 45 nH and peak quality factors of 22 at 100 MHz were achieved for devices embedded in high-resistivity wafers. Devices embedded within standard-resistivity wafers achieved similar inductances but lower peak quality factors of 16 at 40 MHz. Inductors embedded in standard-resistivity wafers also showed lower self-resonant frequencies than their high-resistivity-wafer counterparts. For standard-resistivity wafers, substrate-induced losses are negligible compared to the winding loss at frequencies below 50 MHz, and become dominant above 70-80 MHz. For high-resistivity wafers, substrate and winding losses are comparable at 100 MHz.

Keywords: silicon-embedding, shadow mask, toroidal inductor, substrate-induced loss

INTRODUCTION

Embedding toroidal inductors within the unused volume of the silicon substrate, and potentially implementing through-wafer interconnects to connect the inductors to circuitry on the wafer, is a promising technique to realize ultra-compact power converters. In this approach, the digital control circuitry and power switches are located on the wafer surface while suitable energy storage elements are located within the silicon substrate [1]. Unlike previous embedded spiral inductors [2-3], toroidal inductors constrain the flux primarily within the inductor volume, thereby reducing magnetic interaction with other circuits. Efforts to embed microfabricated solenoid and toroidal inductors have been reported in [4-5] with shallow inductor profiles due to fabrication limitations; these limitations typically lead to low inductance values (e.g., several nH) that are more suitable for RF applications. When considering next-generation integrated power converter systems with operating frequencies of 10-100 MHz, higher inductance (e.g., by increasing the magnetic cross-section) and conductor thickness (to reduce loss) in excess of those achievable by RF inductors are required.

We recently demonstrated an inductor fabrication approach that relies on the use of a 3-D silicon shadow mask to allow for conductor patterning along vertical sidewalls of a silicon recess, resulting in a simplified process for an area-efficient 3-D toroidal

inductor to be embedded into silicon [6]. The inductor has a deep profile and densely-packed electroplated windings to achieve high inductance and low resistance.

Embedding inductors within silicon may result in additional losses at high frequencies, as well as reduced self-resonance frequency, due in part to the parasitics that are introduced by the substrate [1]. The parasitic capacitances mainly arise from the proximity of the winding conductors to the silicon substrate; typically these windings are insulated from the silicon substrate by a thin insulation layer (e.g., PECVD-deposited SiO₂). Without changing the inductor geometry or releasing the silicon underneath the conductors (which is not favored if circuits are to be manufactured on the silicon above the MEMS device), reduction of the capacitance is limited by the maximum insulation thickness that can be practically achieved. Introducing other materials with lower relative permittivity could also reduce these parasitics; however, compatibility with CMOS processes and difficulty of process integration should be considered.

Once the insulation thickness has been maximized, other approaches to reduce the parasitic effects need to be investigated. To understand how substrate resistivity affects the capacitive coupling between the device and the substrate, a simplified equivalent circuit model of the embedded inductor is first proposed and analyzed in Hspice. This model shows

as expected that a high substrate resistivity can reduce parasitic effects. A more comprehensive model based on energy-minimization and Maxwell's equations is then used to thoroughly model the embedded inductor and predict the losses in both the inductor and the surrounding silicon [9]. The effect of using high-resistivity silicon substrates is simulated and compared with the results of using standard-resistivity substrates. Based on these models, inductors in the absence of lossy substrates as well as inductors embedded within silicon wafers of two different resistivities are fabricated, experimentally characterized, and analyzed.

FABRICATION

To realize embedded inductors with sufficient conductor thickness in deep silicon recesses, a shadow-mask-based approach is utilized to enable the bottom and vertical conductors of the toroidal inductor to be formed simultaneously on the recessed surfaces of the silicon trench through one metal deposition and one moldless electroplating process. The top conductors are then formed using a traditional through-mold electroplating technique after the trench has been filled with epoxy for planarization. The specially-designed 3-D silicon shadow mask is formed through a multilevel wafer etching technique and is reusable once fabricated, eliminating multiple photolithography steps and thereby reducing the process time and fabrication complexity.

The detailed process flow for fabricating the embedded inductors using the pre-manufactured shadow mask, as well as the process for generating the 3-D silicon shadow mask, can be found in [6]. Images of the fabricated silicon-embedded toroidal inductors are shown in Fig. 1.

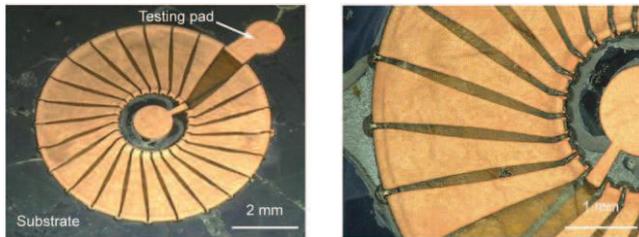


Fig. 1: Images of the fabricated silicon-embedded toroidal inductors. Note the view through the upper windings revealing the bottom windings supported by the oxide-insulated silicon trench etched in the embedding wafer.

MODELING

Simplified Circuit Model

Since embedding the inductor in the silicon substrate introduces substrate effects that may degrade

the device performance, a simplified distributed circuit model is first proposed to understand the capacitive coupling effect between the inductor and the substrate, with one end of the inductor and the silicon substrate being grounded together, as shown in Fig. 2. C_{ox} is the parasitic capacitance between a single copper conductor and the silicon substrate, which is estimated as $C_{ox} = \epsilon A/d$. Since the substrate thickness is comparable to the width of the conductor, the parasitic resistance R_{Si} is estimated from the silicon bulk under adjacent conductors using $R_{Si} = \rho l/A$. The turn-to-turn parasitic capacitance C_{tt} and oxide-to-substrate capacitance C_{Si} is small compared to C_{ox} and therefore is ignored in the simplified circuit model. The values of R_w and L_w versus frequency are obtained from the characterization results of the fabricated inductor with non-silicon substrate [6], which means that R_w and L_w includes the information of inductor loss, but not the substrate-induced loss. Since the number of the turns

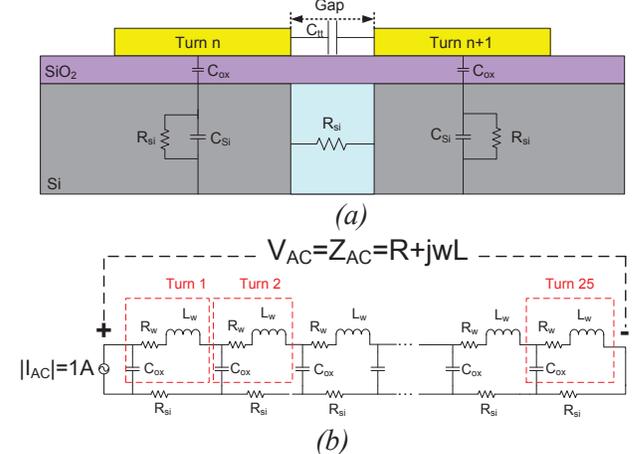


Fig. 2: Schematic illustration of a physical model for a single turn (a) and the simplified distributed model for an embedded inductor that has 25 turns (b).

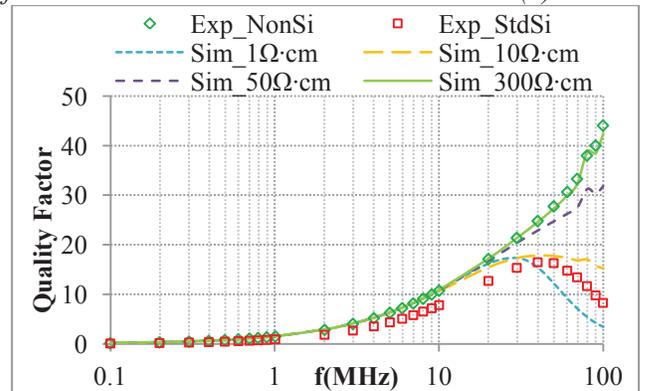


Fig. 3: Simulated quality factor (lines) of the embedded inductors with different substrate resistivities in comparison to the experimental results (symbols) of inductors with non-silicon and standard-resistivity silicon (1-10 Ω·cm) substrates.

in the tested inductor is 25, R_w and L_w is estimated by $R_w = R_{test}/25$ and $L_w = L_{test}/25$. Since the major parasitic effect is expected between the bottom winding and the substrate, the vertical and top windings are neglected.

The simplified circuit model is simulated using Hspice over the frequency range 100 kHz to 100 MHz and the impedance Z_{AC} is calculated, giving the equivalent R and L of the embedded inductor versus frequency. The quality factor of the embedded inductor is obtained by calculating $Q = \omega L/R$, and the results are shown in Fig. 3, and compared with measured results of an inductor in the absence of a lossy substrate and an inductor embedded within a standard-resistivity silicon substrate [6]. Clearly, the simulated quality factor of the embedded inductor in silicon with resistivity of 10 $\Omega\cdot\text{cm}$ matches that of a fabricated inductor in standard-resistivity wafers (1-10 $\Omega\cdot\text{cm}$). The simulated quality factor of the embedded inductor in a substrate of resistivity 300 $\Omega\cdot\text{cm}$ approaches that of the lossless substrate; however, more detailed modeling described below indicates that higher substrate resistivities would be required to approach lossless behavior.

Energy-Method Approach

An analytic model based on energy methods [9] is used to determine the magnetic fields within the embedded inductor, and these fields are used as boundary conditions to a diffusion analysis that determines the winding losses. In this approach, we use several potential functions that are valid over large regions of the inductor to approximate the magnetic vector potential, each function having again a few free parameters. The potential is then used to determine the magnetic energy stored in each region, and the individual stored energies are summed to obtain a total. The values of the free parameters are then determined by minimizing the total stored energy over those parameters. The resulting potentials are finally used to determine the magnetic fields and the winding loss. The end result is analytic expressions for equivalent circuit model parameters that can be examined for physical insight, and rapidly evaluated during iterative design optimization. The equivalent circuit model is also appropriate for circuit simulation. More details can be found in [9].

It is also necessary to model and calculate the additional losses in the surrounding silicon substrate. These include magnetically-driven losses from induced eddy currents, and electrically-driven losses that result from the temporally- and spatially-varying electric potential of each winding turn. To calculate the magnetically-driven losses we assume axial

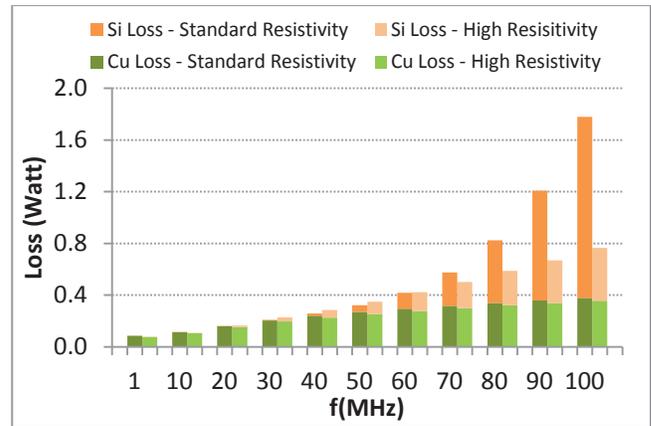


Fig. 4: Calculated copper loss and silicon loss of the embedded inductors using standard-resistivity (1 $\Omega\cdot\text{cm}$) and high-resistivity (5000 $\Omega\cdot\text{cm}$) wafers respectively.

symmetry and solve Maxwell's equations in 1-D. To calculate the electrically-driven losses for a toroid we solve Maxwell's equations in 2-D polar coordinates.

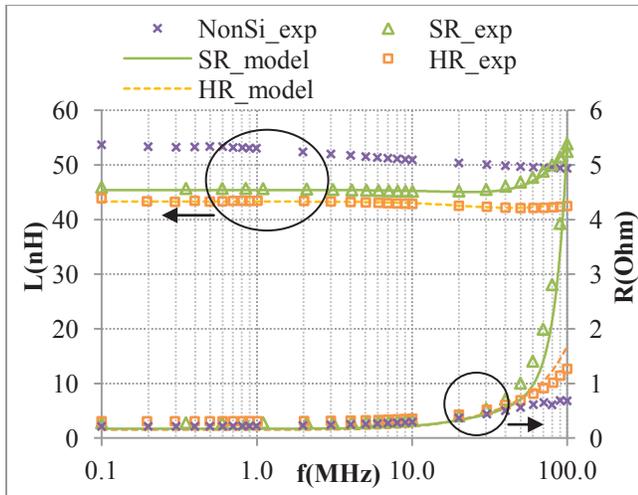
Fig. 4 shows the modeled losses in both the copper windings and the surrounding silicon substrate as functions of frequency. The loss distribution demonstrates that silicon substrate losses are dominant at high frequencies when the inductors are embedded in standard resistivity wafers. This validates the need to use high-resistivity wafers to significantly reduce the substrate losses and improve quality factor at those frequencies. At frequencies below 50MHz, the substrate loss is negligible compared to the copper loss, suggesting that inductor optimization is more important than wafer resistivity in improving device performance.

ELECTRICAL CHARACTERIZATION

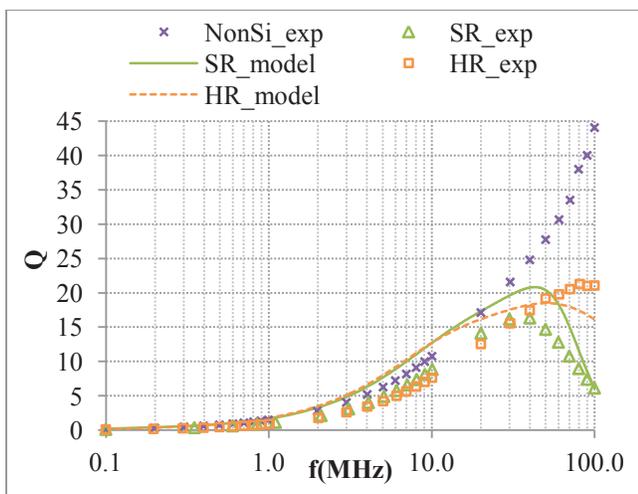
Inductors that are embedded in both standard-resistivity (1-10 $\Omega\cdot\text{cm}$, "SR inductors") and high-resistivity (2000-3000 $\Omega\cdot\text{cm}$, "HR inductors") wafers are fabricated, and inductors with no silicon substrate are also demonstrated in which there are no substrate-induced losses. Electrical characterization of the fabricated inductors was performed using an impedance analyzer (HP4194) and the results are shown in Fig. 5, together with the modeling results from the energy-method approach.

As can be seen from the plots, the modeling results for standard- and high-resistivity wafers are in reasonable agreement with the experimental results. The embedded inductors consist of 25 turns, a height of 300 μm , an outer diameter of 6 mm, an inner diameter of 2 mm, an average copper thickness of 30 μm and an oxide insulation layer of 12 μm . The silicon-embedded inductors demonstrate an

inductance of 45 nH at low frequency and a DC resistance of 300 m Ω . The inductor without silicon substrate exhibits a higher inductance of 53 nH due to the fact that they are fabricated with a slightly larger height. The SR inductor shows resonance effects starting at approximate 50MHz, as can be seen from the inductance result, while the HR inductor demonstrates stable performance up to 100MHz, similar to the inductor with non-silicon substrate. The losses in the embedded HR inductor, as can be seen from the resistance result, are suppressed successfully at high frequencies by using high-resistivity substrates as compared to the SR inductor. The quality factor of the SR inductor reached 16 at 40MHz, while the quality factor of the HR inductor reached 22, in comparison to a quality factor of 45 at 100MHz for the inductor with non-silicon substrate.



(a)



(b)

Fig. 5: Characterization results L , R (a) and Q (b) vs. modeling results for the embedded inductors in standard-resistivity (SR, 1-10 Ω -cm) and high-resistivity (HR, 2000-3000 Ω -cm) wafers.

CONCLUSION

Substrate effects associated with silicon-embedded toroidal inductors that may degrade the inductor performance in the frequency range of interest have been considered based on modeling and experiment. Total inductor losses as well as losses attributable to substrate effects are analyzed using energy-method based models. High-resistivity silicon wafers are shown to suppress substrate loss at high frequency and improve the self-resonance frequency of the embedded inductor.

REFERENCES

- [1] Yu X., Kim M., Herrault F., Kim J.K., Allen M.G. 2012 Silicon-Embedded 3D Toroidal Air-Core Inductor with Through-Wafer Interconnect for On-Chip Integration *Proc. MEMS 2012 (Paris, France, 20-22 January 2012)* 325-328
- [2] Wu R., Sin J.K.O. 2011 A Novel Silicon-Embedded Coreless Inductor for High-Frequency Power Management Applications *IEEE Electron Device Letters* **32** 60-62
- [3] Pan T., Baldi A., Davies-Venn E., Drayton R. F., and Ziaie B. 2005 Fabrication and Modeling of Silicon-embedded High-Q Inductors *J. Micromech. Microeng.* 849-854
- [4] Liang Y. C., Zeng W., Ong P. H., Gao Z., Cai J., and Balasubramanian N. 2002 A Concise Process Technology for 3D Suspended Radio Frequency Micro-Inductors on Silicon Substrate *IEEE Electron Device Letter* **23** 700-703
- [5] Gu L., Li X. 2007 High-Q Solenoid Inductors with a CMOS-Compatible Concave-Suspending MEMS Process *J. Microelectromech. Systems* **16** 1162-1172
- [6] Yu X., Kim M., Herrault F., Kim J.K., Allen M.G. 2012 Silicon-Embedding Approaches to 3-D Toroidal Inductor Fabrication *submitted to J. Microelectromech. Systems*
- [7] Koninck D.A.de, Briand D., Rooij N.F.de 2011 A Shadow-Mask Evaporated PyroMEMS Igniter *J. Micromech.Microeng.* **21** 1-7
- [8] Morishita S., Kim J.H., Marty F., Li Y., Walton A.J., and Mita Y. 2009 A Three-Dimensional Silicon Shadow Mask for Patterning on Trenches with Vertical Walls *Proc. TRANSDUCERS 2009 (Denver, USA, 21-25 June 2009)* 1608-1611
- [9] Araghchini M., Yu X., Kim M., Herrault F., Qiu J., Sullivan C., Allen M.G., Lang J.H. Modeling and Measured Verification of Stored Energy and Loss in MEMS Toroidal Inductors *Proc. ECCE 2012(Raleigh, USA, 15-20 Sept2012)* 3293-3300