SYNCHRONOUS VOLTAGE DOUBLER FOR ELECTROMAGNETIC HARVESTERS

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Abstract: This paper reports on a power conditioning circuit for electromagnetic energy harvesters, based on a two-sided synchronous voltage doubler. The circuit is self-starting in the absence of any auxiliary supply, has a start-up input voltage of 350 mV rms, and can deliver 100 µW of output power with 74% efficiency at the start-up threshold. A novel scheme for controlling the mosfet switching is used which avoids the stability issues that can arise with comparator-based circuits. The circuit was developed for use with a flow-driven energy harvester aimed at duct and pipeline monitoring.

Keywords: energy harvesting, power conditioning, synchronous rectifier, voltage doubler

INTRODUCTION

The design of power conditioning electronics for energy harvesters has received increasing attention in recent years. Miniaturised energy harvesters tend to produce very low levels of output power (often sub-mW), meaning that circuits with ultra-low power overhead are required in order to achieve even modest efficiency levels. Furthermore, depending on the transducer type, the output impedance of the energy harvester may be either very high (electrostatic devices) or very low (electromagnetic), bringing additional circuit design challenges.

The essential function of the power conditioner is to take the raw output of the energy harvester and convert it into the format required by the load, typically a regulated, low-voltage DC supply. However, in many applications the ambient energy source is intermittent and not always able to satisfy the power demands of the load. In such cases an intermediate energy store is required, typically in the form of a battery. The power conditioning problem then becomes one of optimising the flow of power between the harvester, the energy store and the load [1]. In general, the power conditioner should also ensure that the power extracted from the harvester is maximized. In addition to maximum power point tracking in its traditional sense (i.e. electrical impedance matching), this may involve dynamically optimizing the harvester, for example by tuning the mechanical resonant frequency [2].

While most applications for energy harvesters require an energy storage element, there are some where power is required only when the ambient energy source is present, allowing the possibility of battery-less devices. This is an attractive prospect for remote wireless sensing applications where battery replacement, however infrequently it may be needed, is undesirable or impractical. In such applications the demands on the power conditioner are lower because it has only to provide sufficient power for operation of the load; once this level is reached, there is no advantage to be gained by generating higher power levels since excess energy cannot be accumulated. Consequently, in designing the power conditioner the focus can be on maximizing the output power when the ambient source is at its weakest, rather than over the entire operating range. On the other hand, power conditioners for battery-less devices need to be self-starting (or ‘self-priming’) in the absence of an auxiliary supply, and this can be challenging, particularly for electromagnetic energy harvesters which tend to produce low output voltages.

Previous work on power conditioning circuits for energy harvesting has focused on two key building blocks: synchronous rectifiers and low-power DC-DC converters. Synchronous rectifiers using mosfets as active diodes have achieved high efficiencies (≥90%) [3], but operation at input voltages below 1 V has not been demonstrated except in circuits with an auxiliary supply. Self-starting DC-DC converters with exceptionally low starting voltages (down to 20 mV) have also been developed [4], but these do not provide input rectification and tend to have poor efficiency when operated at the lower end of the power range.

The aim of the present work was to develop an efficient, self-starting synchronous rectifier with as low a start-up voltage as possible. A voltage doubler was chosen (as opposed to a simple rectifier) in order to boost the harvester output voltage and thereby relax the start-up voltage requirements imposed on the following regulator or DC-DC converter stage. The circuit was designed specifically for use with the flow-driven energy harvester developed previously at Imperial College and described in [5, 6]. This device consists of a 2 cm-diameter shrouded wind turbine with an integral permanent magnet electromagnetic generator. It was developed as the power source for a battery-less wireless flow sensor aimed at conditioning monitoring in HVAC (heating ventilation and air conditioning) systems.

CIRCUIT OPERATION

Figure 1 shows the circuit investigated in this work. It comprises a pair of classic voltage doublers (C1, D1, C2, D2 and C3, D3, C4, D4) with the four diodes having associated mosfets (M1-M4) to eliminate their forward voltages. The voltage doubler outputs are connected in series, so the open-circuit output voltage (between V+ and V-) is expected to be twice the peak-to-peak open-circuit generator voltage if there are no diode forward drops or other losses.

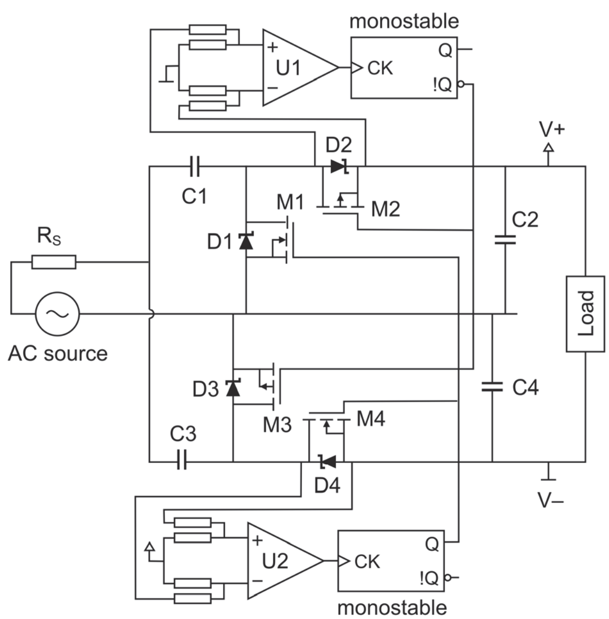

Fig. 1: Two-sided synchronous voltage doubler topology.

Key to the operation of any synchronous rectifier is the generation of appropriate gate drive signals for the mosfets. These must be correctly timed in order for the mosfets to operate effectively as active diodes. In earlier work, reported in [6], we generated the gate drive signals using a manually adjusted pulse-position/width modulator. While this was adequate for an initial study, for real applications a circuit is required that can automatically set the gate timings according to source and/or load conditions.

A common method for controlling active diodes is to use comparators to measure the sign of the diode voltage [3]. However, a difficulty with this approach is that the forward voltage is low when the mosfet is conducting, and consequently the comparator has to detect the zero-crossing of a differential signal with a very low voltage gradient. This can lead to instabilities when trying to turn the diode off. Adding a low-pass filter at one comparator input has been shown to improve stability [7], but this inevitably introduces timing errors and unwanted ripple in the output waveform.

In the circuit of Fig. 1, comparators are used to determine when particular mosfets should turn on. For example, the output of comparator U1 goes high when the bias voltage of D2 crosses zero in the positive direction (assuming equal resistors at the comparators inputs). However, rather than being connected directly to its associated mosfet, each comparator output is used to trigger a monostable which holds the mosfet on for a fixed time interval. When the monostable times out, the mosfet turns off and the sign of the diode voltage is re-tested using the comparator. If it is still positive the monostable is re-triggered; otherwise the mosfet remains off. The monostable period is chosen to be sufficiently short such that the resulting discretization of the gate drive pulse duration has negligible effect on the performance.

The above control scheme could be implemented for every active diode in the circuit. However, in the circuit of Fig. 1 it is applied only to the series diodes, with the resulting gate drive signals also being used to control the shunt diodes. While this is generally non-optimal in terms of voltage doubler performance, it simplifies the circuit, and the loss of efficiency due to timing errors is mitigated by the reduction in power overhead associated with gate drive circuitry.

PROTOTYPE CIRCUIT

A prototype circuit was built using the components listed in Table 1. The mosfets were selected for low threshold voltage, while the diodes used were standard low current Schottky devices. The capacitor values C1-C4 were not fully optimized although PSpice simulations were run to establish the range of values giving best performance in terms of start-up voltage. The comparators were chosen based on their low quiescent current (typically 600 nA) and ability to operate at supply voltages down to 1.6V. A photograph of the prototype circuit is shown in Fig. 2.

Table 1: Key components in prototype.

Part ident	Manufacturer part # and function
M1, M4	Si2302CDS n-channel mosfet
M2, M3	Si2305CDS p-channel mosfet
D1 – D4	BAT54S Schottky diode
C1 – C4	10 μF ceramic capacitor
U1, U2	MCP6541T-I/LT comparator

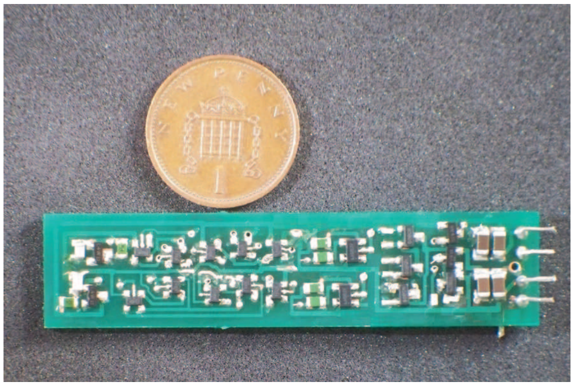

Fig. 2 : Prototype voltage doubler circuit.

The monostables were implemented in SN74AUP series CMOS logic which offers exceptionally low voltage operation (down to 0.8 V) and low static supply currents (typically 0.5 µA per package). Figure 3 shows the schematic of a single monostable. The delay T, which defines the monostable period, was implemented using a simple RC network. The upper feedback path was included to disable the clock input during the monostable cycle; this prevents spurious toggling of the flip-flop due to instability at the comparator output while the mosfet is switching on.

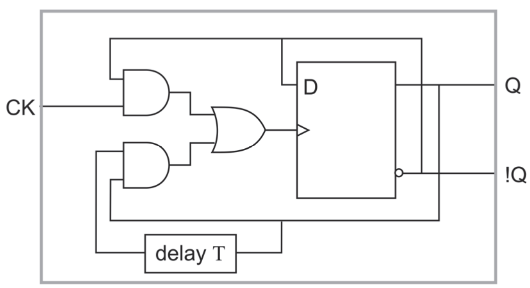

Fig. 3: Discrete logic monostable, implemented in SN74AUP series logic with an RC delay.

The potential divider networks at the comparator inputs in Fig. 1 were included primarily to ensure that the comparator input voltages remain within the allowed common-mode voltage range. However, they also serve another important function. By introducing a slight mismatch in the divider ratios, it is possible to guarantee that the comparator output is stable and low when the mosfet is conducting. The monostable will then only re-trigger at the end of its cycle if the diode voltage moves in a positive direction after the mosfet turns off.

PERFORMANCE

The performance of the prototype voltage doubler was evaluated by feeding it with a sinusoidal input voltage from a signal generator and measuring the average input and output power levels when it was driving a resistive load. The signal generator was set up to emulate the permanent magnet generator of the energy harvester described in [6]. When configured for single-phase operation, this generator has a source resistance of 75 Ω and an open circuit voltage of up to 1.72 Vrms, assuming a maximum turbine rotation speed of 4,000 rpm. The frequency is directly proportional to the open-circuit voltage, with a scale factor of 620 Hz per Vrms.

The input power was calculated off-line, based on captured oscilloscope traces of the input voltage and the voltage across a 25 Ω current sense resistor placed in series with the (50 Ω) signal generator output. The output power was calculated simply as the product of the measured rms output voltage and current values. The load resistor was set to 20 kΩ to give a power consumption in the load of 200 µW at 2.0 V. This value was chosen to allow direct comparison with earlier work reported in [6].

Typical input voltage and current waveforms are shown in Figure 4. Fine structure can be seen in both traces due to the periodic sampling of the current direction in the diodes. This is more prominent in the positive half cycles because the imbalance in the resistive dividers in the upper half of the circuit (due to resistor tolerances) was larger than for the lower half, resulting in slightly longer mosfet off times between monostable cycles. The monostable period was set to around 130 µs.

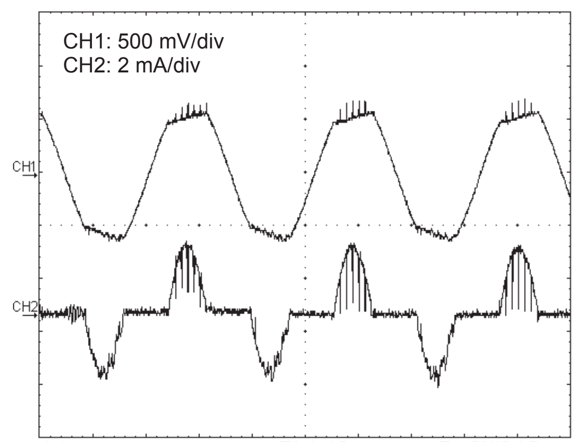

Fig. 4: Input voltage (CH1) and current (CH2) waveforms at an input source frequency of 325 Hz.

Figure 5 shows the voltage transfer characteristic of the active circuit, together with that of a passive circuit based on the same diodes and capacitors. The active circuit displays hysteresis, so curves are included both for increasing (forward) and decreasing (return) input voltage.

The active circuit starts from cold at an open-circuit input voltage of 350 mV rms. The output voltage just before start-up is around 1 V, suggesting that the comparators start to function at a supply voltage some way below the specified minimum. Start-up of the active circuit causes the output voltage to rise suddenly to 1.4 V, at which point the circuit is delivering ~100 μW into the load. Once the circuit is running, it will continue operating at open-circuit input voltages down to 300 mV rms.

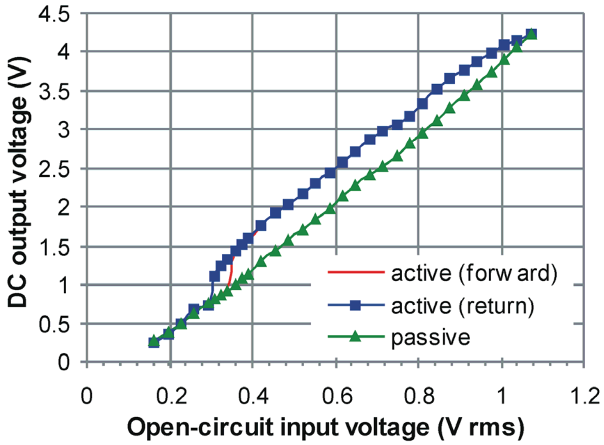

Fig. 5: Measured voltage transfer characteristics for active and passive circuits with 20 kΩ load. The forward and return curves for the active circuit coincide except around the hysteresis loop.

Figure 6 compares the efficiencies of the active and passive circuits. The active circuit achieves higher efficiency at low input voltages, which was the primary objective in this work. The efficiency at the start-up threshold is 74%, implying a power overhead of only ~35 μW

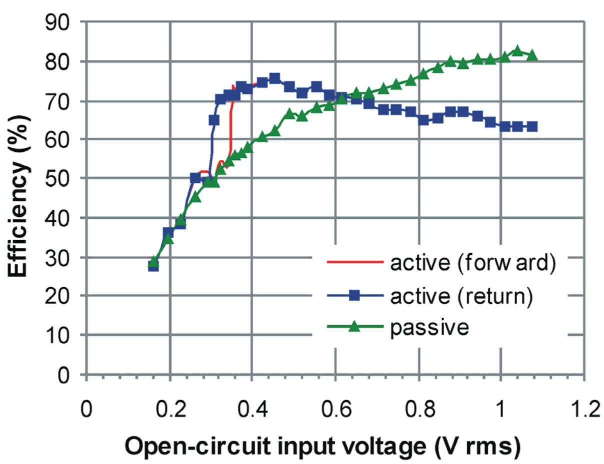

Fig. 6: Measured variations of efficiency with AC input voltage for active and passive circuits.

The active circuit performs less well at higher input voltage levels, and is actually less efficient than the passive circuit for input voltages above 620 mV rms. This is because the dynamic power consumption of the gate control electronics increases with supply voltage and frequency. There is scope for reducing this, both by circuit improvements and by regulating the supply to the gate control circuits.

CONCLUSIONS

A self-starting, synchronous voltage doubler has been demonstrated which offers low start-up voltage and high efficiency at power levels as low as 100 μW. A novel approach has been used to ensure robust control of the mosfets in the active diodes. The use of a voltage doubler topology relaxes the start-up voltage requirements of the subsequent regulator stage.

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