

# FULLY MONOLITHICALLY FABRICATED Si ONE-CHIP MINIATURE FUEL CELL

## -CHEMICAL MODIFICATION OF POROUS Si FOR PROTON CONDUCTIVITY-

Ryohei Ogawa<sup>1</sup>, Shin Aoki<sup>1</sup> and Masanori Hayase<sup>1</sup>  
<sup>1</sup>Tokyo University of Science, Noda, Chiba, Japan

**Abstract:** A formation process of electrolyte layer was proposed for our one-chip miniature fuel cell. In the one-chip miniature fuel cell, a porous Si layer between catalyst layers is required to work as electrolyte. Therefore, we studied about chemical modification of pore wall surface with sulfonic acid. By the chemical modification, the porous Si is expected to have ion conductivity and work as electrolyte layer of the one-chip fuel cell. The modification process was carried out, and the processed specimen was characterized by Energy Dispersive X-ray spectrometry, Fourier Transform Infrared Spectrometry and AC impedance method. These results suggest that the modification process was successfully carried out, and pore wall surface obtained ion conductivity.

**Keywords:** fuel cell, porous silicon, MEMS, chemical modification

### INTRODUCTION

Fuel cells have attracted large attention as ultimate portable power sources and many research groups have studied about miniaturization of fuel cells [1-10]. In the last PowerMEMS 2011, we reported the fully monolithically fabricated Si one-chip fuel cell as shown in figure 1 [11]. The one-chip fuel cell does not need hot-pressing process. The fabrication process is well suited to MEMS batch process, and is advantageous to mass productivity. Generally, PEM (Polymer Electrolyte Membrane) is used for the electrolyte layer. In the one-chip miniature fuel cell, a porous Si layer between catalyst layers is required to work as an electrolyte [12][13]. In the prototype cell, we reported last year that Nafion solution was immersed into the porous Si layer, and the electrolyte layer was prepared. Power generation was successfully demonstrated by the prototype cell, though the observed OCP (open circuit voltage) of the prototype cell was only 470mV. This result suggests that serious fuel cross over happened through the electrolyte layer.

In our previous report, demonstration of the power generation was focused, and the electrolyte layer formation was quite preliminary. Pichonat et al. reported that the good performance was not easily available by filling Nafion solution into the porous Si. Novel approach for the electrolyte layer formation is needed.

Moghaddam et al. employed a chemical modification on the porous Si wall surface, and good performance was demonstrated. The modification approach seemed quite promising, and various studies

will be needed.

In this study, we propose a novel modification process, and the modified porous Si was characterized by EDX (Energy Dispersive X-ray spectrometry), FT-IR (Fourier Transform Infrared Spectrometry) and AC impedance method.

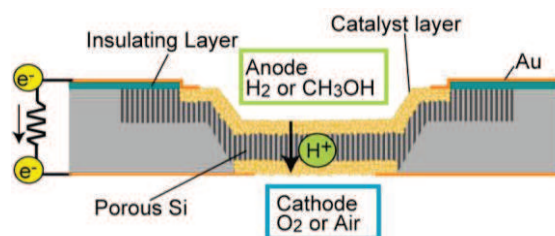


Figure 1: Schematic of the one-chip miniature fuel cell.

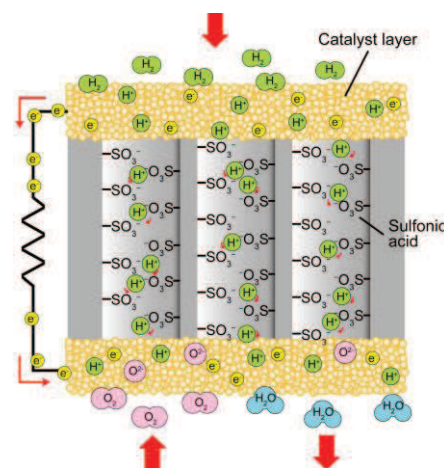


Figure 2: Chemically sulfonated porous Si layer working as an electrolyte layer.

## EXPERIMENTS

The Si wafers used in this work were n-type, 110 $\mu\text{m}$  thick, (100)-oriented, mirror-polished on both sides and P-doped 0.008-0.02  $\Omega\text{cm}$  resistivity. Thermally oxidized film was formed on both sides. Si wafers were cut into small pieces of 15 mm square.

### Through-chip porous layer

Using photolithographic patterning and wet etching, rectangular pits are formed on a Si chip as shown in figure 1. About 60 $\mu\text{m}$  is etched on the pits area, and the remaining thickness from the bottom of the pit to the opposite side become 50 $\mu\text{m}$ . After removal of thermal oxide film by HF solution, anodization in a HF containing solution is performed on the pit side, and porous Si is formed. Anodization is stopped a few  $\mu\text{m}$  before the porous layer reached the opposite side. The remaining bulk Si crystalline of a few  $\mu\text{m}$  thick is removed by reactive ion etching (Samco RIE-10N). It is known that the porous Si layer has a small pore region on the top of the porous Si layer. In order to remove the small pore region, the pit side of the chip is also slightly etched. Finally, through-chip porous Si layer is obtained. Figure 3 shows the appearance of the chip. 6 pits were formed, and the diameter of the porous Si area, which is seen as dark circle in the left image, was about 9mm.

### Chemical modification process

Organic synthesis process was applied for the pore wall modification. Proposed scheme is shown in figure 4. At first, hydrophilic Si-OH surface was prepared on a Si chip with through-chip porous Si layer by short thermal oxidation. Then, the chip was immersed into a 10mM of APTES (3-aminopropyltriethoxysilane) solution with toluene

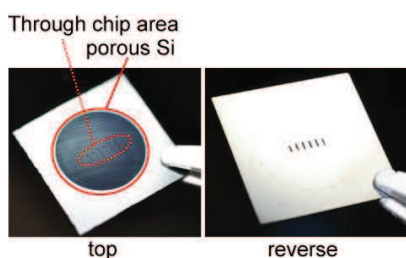


Figure 3: Appearance of the Si chip with the through-chip porous Si layer.

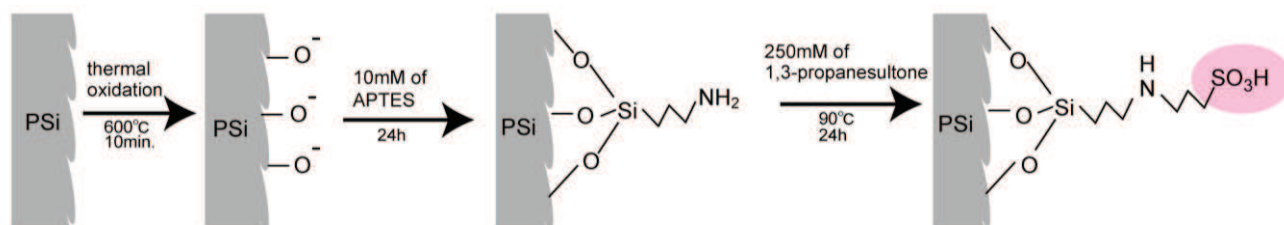


Figure 4: Scheme of the sulfonation on the porous Si pore wall.

solvent for 24 hours, and amine is linked to Si pore wall surface[14][15]. Finally, the chip was immersed into a 250mM of 1,3-propanesultone solution with acetonitrile solvent at 363K for 24 hours. It is expected that the amine reacts with the 1,3-propanesultone, and the sulfonic acid is linked to the pore wall surface.

### Characterization

The chemically modified porous Si was characterized with three methods. At first, as the easiest method, EDX analysis is performed. Characteristic elements, such as N and S are focused. Then, the specimen is analyzed by FT-IR, and some characteristic molecular structures are sought. Finally, ion conductivity is measured by AC impedance method.

## RESULT AND DISCUSSION

### EDX elemental analysis

Top side of the chip was observed by SEM with EDX (Hitachi S4200). Specimens were measured after APTES process and complete sulfonation process, respectively. Figure 5 shows the EDX spectra on the porous layer. It is found that strong S signal is observed after the sulfonation, while no S signal is observed at the APTES process. The S signal is assumed to reflect the sulfonic acid. Though oxygen signal became smaller after the sulfonation,

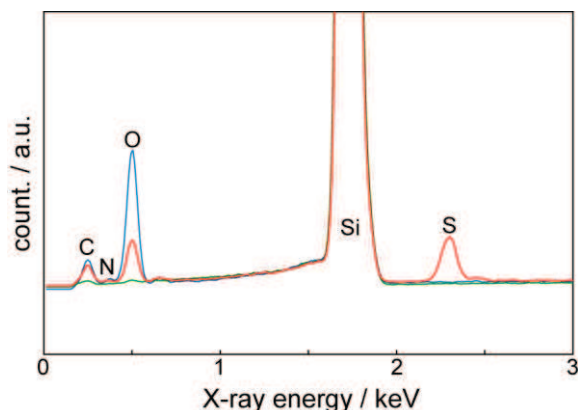


Figure 5: EDX spectra at each process step: (red) porous Si surface after the sulfonation (blue) porous Si surface after APTES process (green) flat area of the chip after the sulfonation.

elimination of oxygen contamination is difficult. At this point, we considered that the oxygen signal does not reflect the modification process. Though slight N signal was observed, the signal was not significant, and we did not use N signal for the characterization.

Figure 5 also shows the spectra on flat area of the chip, where anodization is not applied, and the porous Si layer after the sulfonation process. In the process, whole chip was immersed into the process solution, and flat area is also assumed to be modified. The result show no S signal on the flat area. It is supposed that the porous area had large surface area, and the signal became larger. Therefore, it is supposed that the modification process successfully penetrated deeply into the porous Si layer.

### Infrared adsorption analysis

The specimen chips were measured by FT-IR with transmission mode. FT-IR can detect chemical bonding state. Therefore, modification process of sulfonic acid can be confirmed.

Figure 6 shows result of FT-IR spectra. Dot line shows the spectrum of a specimen after the APTES process. Solid line shows the one after the complete sulfonation process. Unfortunately, sulfonic acid signal, which is expected to appear around  $1350\text{cm}^{-1}$ , was hidden by strong Si-O signal. Therefore, direct measurement of the sulfonation was not possible.

Then, we focused on amine part. It was found that a  $\text{NH}_2$  vending vibration signal appears at  $1600\text{cm}^{-1}$  due to APTES before sulfonation, while the  $\text{NH}_2$  signal decreased after the sulfonation. After sulfonation, a  $\text{NH}$  vending vibration signal appears at  $1650\text{cm}^{-1}$ . After the reaction of 1,3-propanesultone with the amine,  $\text{NH}$  is expected to appear as shown in figure 4, it suggest that the reaction occurred successfully.

Around  $3400\text{cm}^{-1}$ , small peak was generated after the sulfonation process. The peak is assumed to be due to of O-H stretching vibration at the sulfonic acid. These results support the success of the sulfonic acid modification.

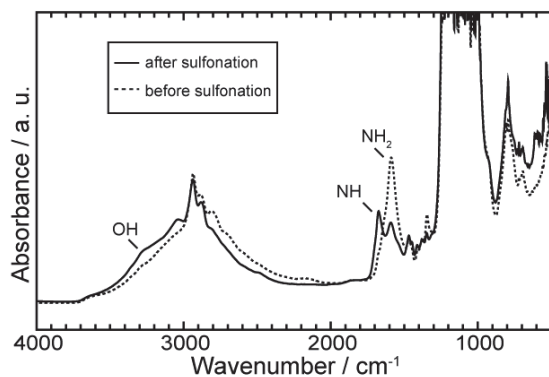


Figure6: FT-IR spectra before and after the sulfonation.

### Result of AC impedance

Above analysis suggested that the sulfonic acid was successfully linked to the pore wall surface. Finally, ion conductivity was roughly estimated by the AC impedance method. Dimension of specimen is quite small compared to usual PEM sheets, besides the shape is not simple sheet. The porous layer is fragile. Usual conductivity measurement needs large cramping force [16], and it is difficult to apply usual impedance measurement to our specimen.

In order to reduce the cramping force to the specimen, gold was sputtered on the both sides of the porous Si layer for electric connections as shown in figure 7. Crystalline Si has large conductivity, and it causes electric short if the gold was simply sputtered on both sides. Therefore, regarding the porous Si as an insulator, we limited the gold sputtered area as shown in left image of figure 7.

Specimen chips at each process step and conventional Nafion filled chip were prepared, and totally four specimens were measured. All chips were acidified in a  $1\text{M H}_2\text{SO}_4$  solution for 1 hour and were carefully rinsed by ultrapure water. Before the measurement, ultrapure water was dropped on the Au layer on the chips to wet the porous layer.

Resistance of the chips was determined with the Nyquist plot as shown in figure 8. Real part of the impedance at 1 MHz was considered as the resistance. The resistance decreased along the sulfonation process steps. After the APTES process, it was assumed that

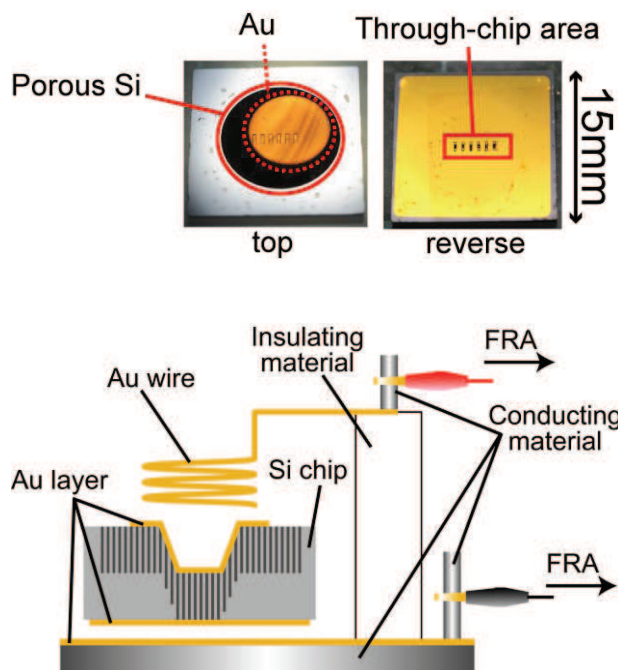


Figure7: Experimental setup for the AC impedance measurement. Gold film was sputtered on the chips.



Table 1: Estimated ion conductivity of chemical modified porous Si.

Specimen	Resistance of Si chip	The ion conductivity
Porous Si after thermal oxidation	$1.8 \times 10^3 \Omega$	$8.0 \times 10^{-6} \text{ S/cm}$
Porous Si immersed APTES	$6.5 \times 10^1 \Omega$	$2.2 \times 10^{-4} \text{ S/cm}$
Porous Si immersed 1,3-propanesultone	$1.3 \times 10^1 \Omega$	$1.1 \times 10^{-3} \text{ S/cm}$
Nafion filled chip	$3.2 \times 10^0 \Omega$	$4.6 \times 10^{-3} \text{ S/cm}$

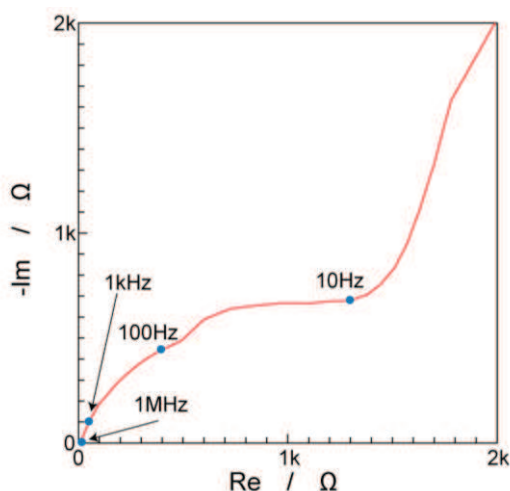


Figure8: Nyquist plot of porous Si after the sulfonation.

NH<sub>2</sub> contributed the ion conductivity. As we expected, further reduction of the resistance was obtained after the sulfonation. Ion conductivity was estimated assuming that the ion conductivity was uniform under the gold sputtered area of 6.6 mm in diameter and the outside of the gold area did not contribute to the conductivity.

Unfortunately, the ion conductivity of the sulfonated porous Si was lower than the conventional Nafion filled one. It is assumed that the conductivity is largely depends on the real surface area of the porous Si layer. Morphology of porous Si can be tunable and further optimization will be available. Although the conductivity was not adequate at this point, the same order of conductivity as bulk Nafion ( $10^{-1}$  to  $10^{-3}$  S/cm) was obtained. Combination with other methodology is also applicable, and further study will be continued.

## CONCLUSION

In this study, chemical functionalization of porous Si was discussed, and the sulfonation of the pore wall was demonstrated by a simple organic synthesis process. The modification process was ascertained at each step by EDX, FT-IR and AC impedance method. The AC impedance showed ion

conductivity of  $1.1 \times 10^{-3}$  S/cm. Though the value is not adequate, there is a log of rooms for improvement. Further study will be performed for the ion conduction of porous Si layer.

## Acknowledgment

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