MINIATURE FUEL CELL WITH MONOLITHICALLY FABRICATED Si ELECTRODES -REMOVAL OF RESIDUAL POROUS Si ON A CATALYST LAYER-

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Abstract: The impact of residual porous Si on a porous Pt catalyst layer on fuel cell performance was investigated. In our miniature fuel cells, a catalyst layer is synthesized on a Si chip by changing porous Si to porous Pt with wet plating process. Due to some technical limitations in the fabrication process, porous Si is left on the porous Pt layer. This residual porous Si has bad impact on the performance by blocking fuel supply. In this study, the impact of the residual porous Si was experimentally examined and it was found that the residual porous Si lowered the performance.

Keywords: MEMS, fuel cell, PEFC, porous silicon, porous Pt, plasma etching

INTRODUCTION

Portable electronic devices have driven research about small electric power sources. At this point, Li ion batteries are widely used in the portable devices, and a demand for higher electric energy storage is increasing for higher functionalities. Thus, fuel cells have attracted large attention as ultimate portable power sources [1].

Many prototype miniature fuel cells have been reported, and a few products were put in the market experimentally. But, there are no miniature fuel cells available in a usual consumer market yet. Production cost and mass productivities may be the reason, besides further miniaturization is still needed. MEMS fabrication technology is an important tool to reduce the fuel cell structure to micrometer scales and is advantageous for mass production. Therefore, various studies using Si substrate and MEMS techniques have been performed [2-9].

We have studied a thin polymer electrolyte membrane (PEM) fuel cell with monolithically fabricated Si electrodes. Figure 1 illustrates our fuel cell structure. The porous Pt layer, which works as a catalyst layer, is synthesized on a Si chip. After the porous Pt layer formation, plasma etching is applied, and fuel channels are opened. A PEM sheet is hotpressed with two Si electrodes, and production of a fuel cell is completed. Thickness of the Si wafer is about 100μm and the total thickness of a cell is less than 230μm. Prototype cell showed a relatively high output of 480mW/cm^2 among MEMS based fuel cells.

Though the maximum power density is high, the performance varies largely with each cell. Due to some technical limitations in the fabrication process, porous Si is left on the porous Pt layer frequently as shown in figure 2. We suspected that this residual porous Si had bad impact on the fuel cell performance by blocking fuel supply to the catalyst layer. In this study, the residual porous Si was reduced, and the impact of the residual porous Si was discussed.

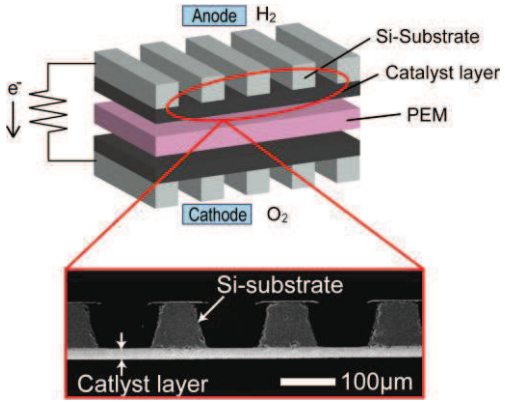

Fig. 1: Schematic view of the miniature fuel cell and the cross section of the monolithic Si electrodes.

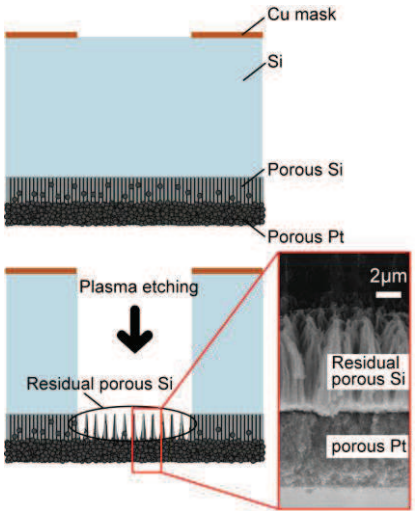

Fig. 2: Residual porous Si layer.

EXPERIMENTS

Si Electrode

Figure 3 illustrates the fabrication process of the Si electrode. The electrode chip has quite simple structure, in which a catalyst layer and fuel channels are monolithically fabricated on a Si wafer. A highly doped Si wafer, that has low resistivity, works as a current path. After removing oxide by HF, copper thin film is deposited on the Si wafer by sputtering. Using usual photolithographic patterning with photoresist and wet etching, fuel channel mask for plasma etching is made with the copper thin film. Porous Si layer is formed on the opposite side of the Si wafer by anodization in an electrolyte containing HF. The porous Si layer is subsequently submerged in a Pt plating bath, and porous Pt layer is obtained. Detailed formation process is described in ref. [10]. Fuel channels are opened by applying plasma etching on the backside of the porous Pt layer with the cupper thin film mask.

Conventional parallel plate reactive ion etching system (Samco RIE-10N, Japan) is used and 18sccm of SF_6 and 4sccm of O_2 gases are supplied for the etching [11]. In this plasma etching process, porous Pt layer is supposed to work as a stopping layer of the etching, because the etching rate is low at the porous metal layer, and through-chip porous Pt layer can be relatively easily fabricated. In this way, monolithic Si based electrodes were prepared.

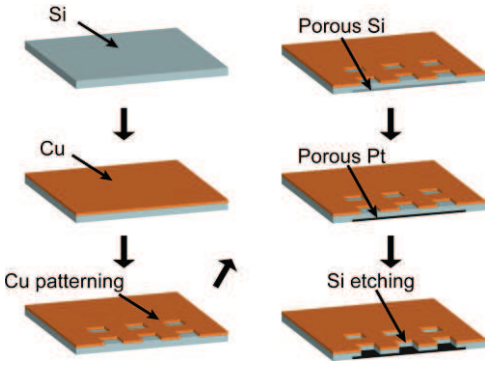

Fig. 3: Fabrication process of the Si electrode.

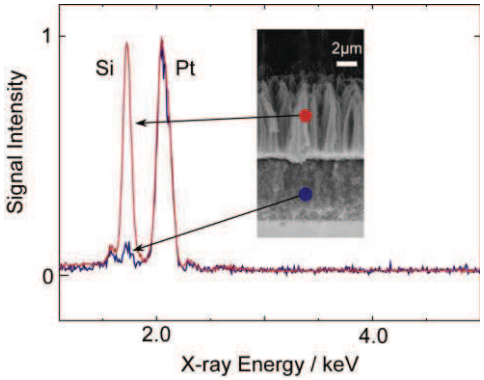

Fig. 4: EDX spectra of the porous layer.

Residual Porous Si

Figure 2 illustrates the residual porous Si. We suspect that the residual porous Si has bad impact on the fuel cell performance by blocking fuel supply to the catalyst layer. No residual porous Si was desired, but it was not easy to remove the residual porous Si completely by plasma etching. The Energy Dispersive X-ray spectrometry (EDX) spectra on the porous layer are shown in figure 4. The residual porous Si region and porous Pt rich region were analyzed. The spectra were normalized with Pt peaks. A red line shows the spectrum on the residual porous Si, and a blue line shows the spectrum on the porous Pt. Only small Si signal was observed at the Pt rich region as we previously reported, while Pt signal intensity was almost same as Si on the residual porous Si region. Though Pt deposit was hardly observed on the residual porous Si region with SEM observation, it was revealed that Pt deposited inside the residual porous Si layer.

We had attempted to remove the residual porous Si layer by extra etching time, and it was found that etching progress was strongly suppressed at the residual porous Si region. Therefore, the removal of residual porous Si by plasma etching was failed in.

Table 1: Condition for the catalyst layer formation.

Property of Si substrate	
Crystal Orientation	(100)
Type	N
Thickness of Si substrate	100μm
Resistivity [Ωcm]	0.001-0.003
Anodization condition	
Composition of solution	Water:HF(46%):Ethanol=5:3:2
Pt immesion plating condition	
Composition of solution	20mM H_2PtCl_6 + 1M H_2SO_4 + 450mM HF
Plating time [min]	15
Temperature [K]	283

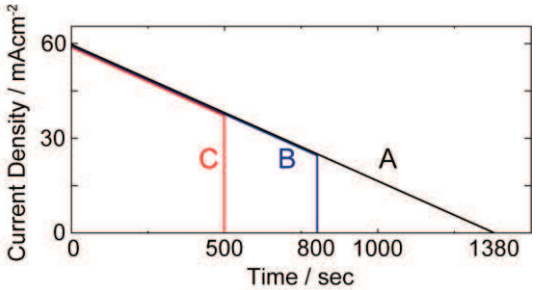

Fig. 5: Modulation of anodization current.

Approach for Reducing of Residual Porous Si

Thickness of the porous Si layer is not strictly proportional to the anodization charge. Besides, the morphology of the porous Si depends sensitively on the resistivity, which varies even in a wafer. Therefore, strict thickness control of the porous Pt layer was not easy, and our attention was mainly given to process conditions to enable stable production. A lot of efforts with trial and error were made to find the process conditions, and table 1 shows the conditions used in recent studies. For the formation of porous Si layer, we have chosen the current modulation in which anodization current was reduced linearly during 1380 s from 60mA/cm^2 to zero. With this condition, thickness of the obtained porous Si layer was excessive to the desired catalyst layer thickness to ensure the mechanical strength of the chip, and we neglected the impact of the excess porous Si. However, recent studies suggested the blocking of fuel supply and difficulty of the removal of the residual porous Si.

In order to reduce the residual porous Si, it is considered that reduction of the original porous Si layer thickness is the simplest way. Therefore, the anodization time is shortened, and the effect of the porous Si layer thickness on the catalyst layer formation was examined. Three conditions as shown in figure 5 were tested. Condition A shows the present condition we have used. With conditions B and C, anodization time was shortened and current was stopped at 800 s and 500 s, respectively. The 500 s anodization time was determined by some preliminary experiments. Pt deposition conditions were not changed, and the conventional 15 min immersion plating was performed.

RESULT AND DISCUSSION

Removal of Residual Porous Si

Cross sectional SEM images of the porous Si layers are shown in figures 6. Thickness of the porous Si layer is reduced by shortening the anodization time. The thicknesses of the porous Si layers with conditions A to C were a 25μm, 20μm, and 13μm, respectively. The current charges of condition A to C were 41.4 C/cm^2, 34.1 C/cm^2, and 24.6 C/cm^2, respectively. It was reconfirmed that the thickness of the porous Si is not proportional to the applied anodization charge.

SEM observation was performed after the plasma etching process. Figure 7 shows the cross section of the catalyst layer and the bottom of the fuel channel, where the plasma etching reached the catalyst layer. It is found that the residual porous Si layer was successfully reduced by the shortening of the anodization time as we expected. Though many irregular fragments were observed on the porous Pt layer in the cross sectional image (figure 7(a)), the bottom image (figure 7(b)) shows few fragments. In the cross sectional image, some objects far behind the real cross section can be observed because of the SEM's large depth of field. Therefore, it is assumed that almost no residual porous Si layer was realized in the condition C.

Power Generation Test

Reduction of the residual porous Si layer was succeeded in. The effect of the residual porous Si layer on the fuel cell performance was discussed. Prototype fuel cells were assembled with Si electrodes fabricated with the above three different conditions. The PEM used in the prototypes was a SF-150 (Toagosei Co. Ltd. , Japan).

The prototype cells were put in an aluminum casing, and 8 sccm of hydrogen gas and 4 sccm of oxygen gas were fed into the cells in a temperature controllable chamber at 318K. In order to obtain good ion conductivity of PEM, hydrogen gas was humidified by bubbling through a water containing tank which was heated at the testing temperature.

In order to grasp the reproducibility of the cell fabrication process, at least, three prototypes were

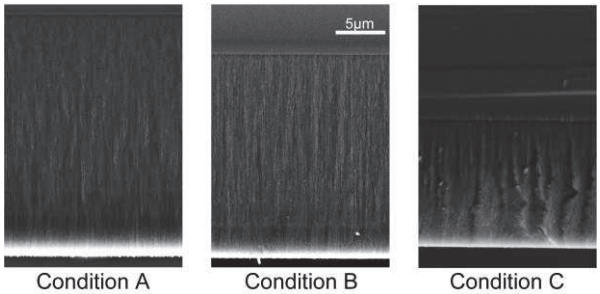

Fig. 6: Cross sectional SEM images of the porous Si layer.

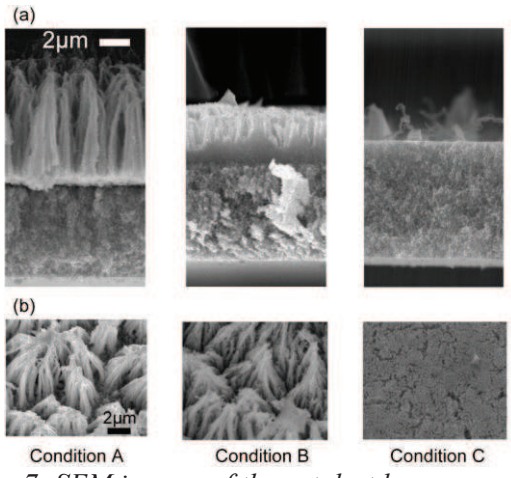

Fig. 7: SEM images of the catalyst layers. (a): Cross section. (b): Fuel channel bottom.

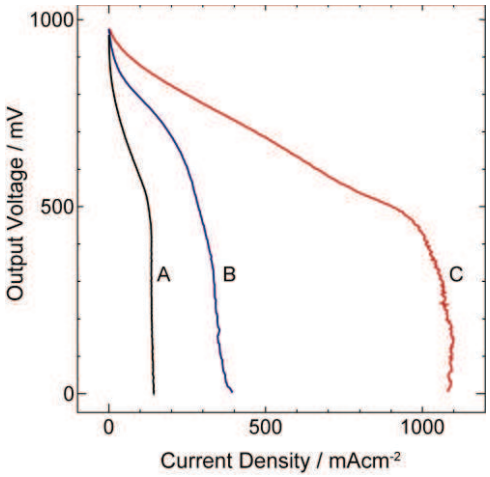

Fig. 8: Typical polarization curves of the cells made with the three different conditions.

prepared on each process conditions, A - C. Typical polarization curves are shown in figure 8. Figure 9 shows the comparison of maximum output power with the three process conditions. Error bar shows the maximum and minimum outputs obtained by different prototypes prepared by identical process conditions. It is found that output increased with residual porous Si layer decrease.

In figure 8, all cases show steep voltage drops around 500 mV, and it is suggested that flooding happened around the voltage. Current density, which causes the flooding, varied largely. It is suggested residual porous Si is easily filled with water and blocks the fuel supply.

There is also significant difference at higher voltage, where the current density is small and the water generation is small. With residual porous Si, the current density was lowered significantly. This suggests that the residual porous Si blocks the fuel gas supply even in a dry condition.

It was clearly demonstrated that the residual porous Si had a bad impact, and the removal of the layer successfully realized higher output. However, prototype cells made with the identical fabrication conditions showed still large variation in performance. We need to find out the factor of the large variation for further improvement.

CONCLUSION

The effect of anodization condition on residual porous Si was experimentally investigated. Three anodization conditions were tested. Shortening the anodization time reduced thickness of the porous Si layer, and the catalyst layer without residual porous Si layer was realized.

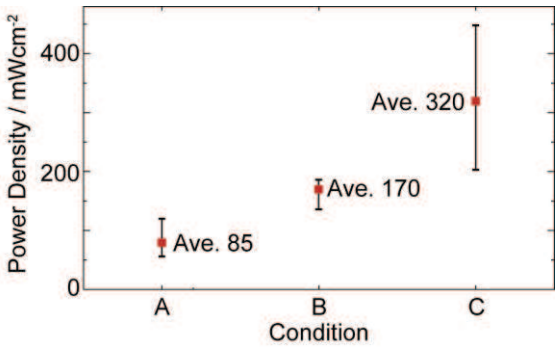

Fig. 9: Comparison of maximum output power

The effect of the residual porous Si layer on the cell performance was also investigated. Power generation test showed that the residual porous Si layer lowered the cell performance significantly, and good performance was demonstrated by removing the residual porous Si layer.

There is still large variation in performance. Further study will be performed to find out the factor of the large variation.

Acknowledgment

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