DESIGN AND FABRICATION OF A MEMS THERMOELECTRIC GENERATOR FOR ENERGY HARVESTING

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Abstract: This paper presents a technology platform to fabricate micro thermoelectric generators (µTEG) with thin-film thermopiles. The combination of bulk and surface micromachining processes allows the integration of in-plane thin-film thermopiles in a device with a cross-plane heat flux. Heat flux guiding structures are used to maximize the temperature difference across the thermopiles. FEM simulations indicate that up to 94% of the total temperature difference applied across the generator chip is located between the thermocouple junctions. A demonstrator device and test structures are manufactured using n-type poly-Si and Al as active materials. Measurements show a linear output voltage of 76.08 μVK^{-1} per thermocouple which would result in a device power factor of $1.612 \cdot 10^{-4}$ $\mu Wmm^{-2}K^{-2}$.

Key Words: energy harvesting, thermoelectric generator, thermopiles, Seebeck effect

1. INTRODUCTION

In modern technological systems, there is an increasing demand for distributed sensor networks. Ideally these sensor nodes communicate wireless and are energy autonomous. Batteries, which are the common sources of energy for such systems, suffer from their relatively large size and heavy weight and also have a limited lifetime. To overcome these shortcomings, ambient energy harvesting is proposed [1]. Besides the conversion of mechanical energy into electrical energy via electrostatic [2], piezoelectric [3] or electromagnetic effects [4], the (waste) heat recuperation via the thermoelectric effect is intensively studied [5, 6, 7].

This paper describes the design, fabrication and characterization of a thin-film thermoelectric generator with optimized heat flow path, so that a maximum temperature difference is located between the thermocouple junctions. The meandering thermocouples (n-poly-Si/Al) are fabricated on a Si wafer in thin-film technology to achieve a high integration density. The heat flux is introduced vertically over the foot-print area of the chip, guided through the thermocouples in a planar direction, and released vertically over the foot-print area. This arrangement guarantees a maximum thermal coupling of the generator to the environment and a maximum temperature gradient across the thermocouples. The fabricated devices are tested and compared with simulation results.

2. DESIGN AND SIMULATION

Fig. 1 schematically depicts the design of the generator, which is combined from three independent fabrication modules. Module A concerns the thermoelectric structure, basically, a rectangular meander of the thermocouple materials deposited on a Si wafer. A barrier layer of SiO_2 insulates the thermopiles to prevent electrical short-circuit by the thermal contact structure fabricated in module B. This concept allows to employ all kinds of thermoelectric materials that can be deposited on a Si substrate. For a functional prototype, n-doped poly-Si and Al are chosen, due to their availability in the in-house clean-room facilities. Other materials, such as n-/p-poly Si or BiSbTe-alloys would lead to a better performance. A single device with $10x10mm^2$ in size carries 7500 thermocouples with a length of 120 µm. Module B includes the thermal connectors on top of the thermoelectric structure that conduct the heat from the top surface to the hot thermocouple junction. For this purpose, metal is deposited within trenches formed by thermally insulating SU-8 photoresist. The large metal area on top serves as thermal contact pad. In module C, the hot junction is thermally insulated from the substrate by a back-

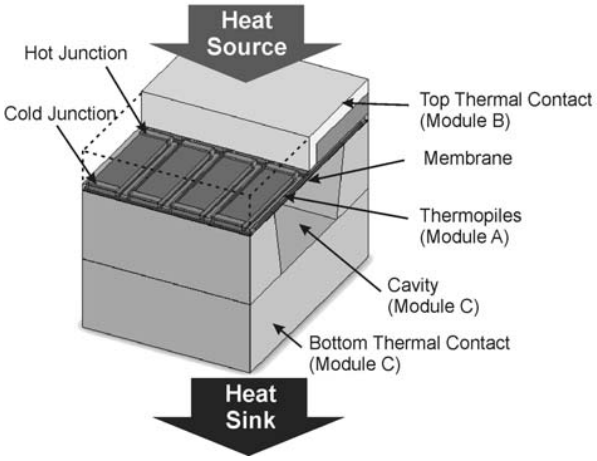

Fig. 1: Schematic of the thermoelectric generator indicating the different fabrication modules.

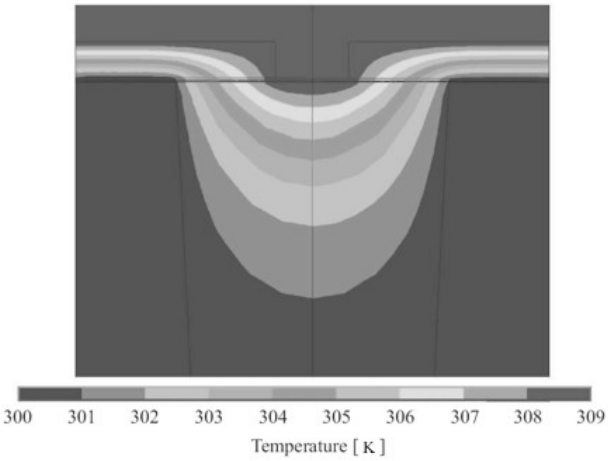

Fig. 2: Temperature distribution within the thermoelectric generator obtained by a 2D FEM thermoelectric simulation with ANSYS.

side DRIE process through the substrate. In this way, the cold junction is thermally connected with the bottom, cold side of the generator. A second wafer is bonded to the back side to realize a good thermal contact and to avoid cavity contamination.

A 2D model of one thermocouple pair is used for thermoelectric FEM simulations with ANSYS, see Fig. 2. The results are extrapolated to a chip of 10x10mm² size with 7500 thermocouples. A temperature difference of 10 K across the entire chip yields an open-circuit voltage of 7.46 V and a maximum output power of 36.3 µW. To compare the result with other devices, the so- called power factor is commonly used [8]. With the results above a power factor of $3.63 \cdot 10^{-3}$ $\mu W m^{-2} K^{-2}$ is calculated. The effective temperature difference between the thermocouple junctions is determined to 9.37 K, which is 93.7% of the total temperature difference. Furthermore, the simulation allows to calculate the thermal resistance of the device which is 1.555 K/W. The electrical resistance is calculated to be 383 kΩ.

3. EXPERIMENTAL

3.1 Material Characterization

The performance of thermoelectric devices is directly linked to several material properties. Therefore test structures have been developed to allow wafer-level testing of the thermoelectric properties of the active material. Van-der-Pauw test structures allow measurement of the electrical resistivity of Al (0.04303 ± 0.111 µΩm) and poly-Si (6.294 ± 0.204 µΩm). The membrane-based test structures depicted in Fig. 3 are used to measure the Seebeck coefficient of the material pair n-poly Si / Al which is found to be 106.18 ± 4.63 $\mu V K^{-1}$.

3.2 Device Fabrication

The fabrication of the device starts with Module A, the thermocouple structure. Thermal SiO_2 and LPCVD Si_3Ni_4 are subsequently deposited on a 300 µm thick 4-inch wafer. Afterwards, 700 nm n-doped poly-Si are deposited by LPCVD and structured by plasma etching. The remaining poly-Si bars are covered

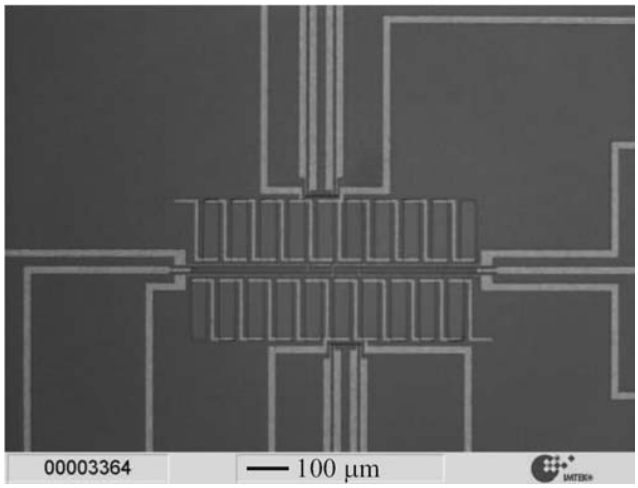

Fig. 3: Microscopic image of the membrane based test structure to measure the Seebeck coefficient.

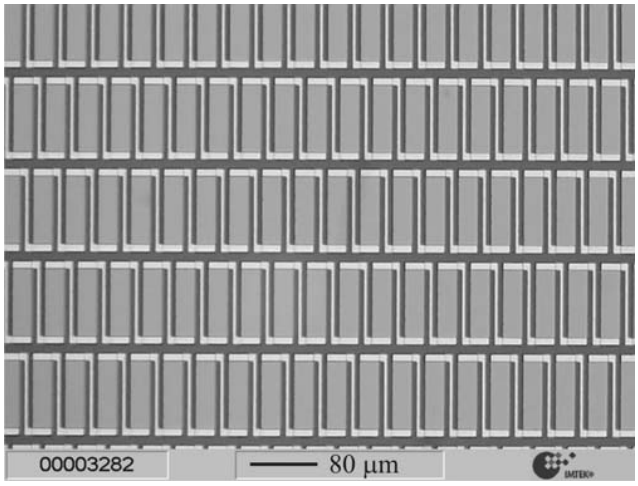

Fig. 4: Microscopic image of the meandering thermocouple structure.

with a 250 nm Al layer. Wet etching of the Al layer leads to the meandering thermocouple structure depicted in Fig. 4. For electrical insulation a 1200 nm thick layer of PECVD SiO_2 is deposited on top. The fabrication of the upper thermal contact structure (Module B) starts with the deposition of a Cr/Au seed layer for the electroplating process. The seed layer is structured by wet etching. An SU-8 photolithography creates the grooves that are filled electrochemically with Au afterwards. A second seed layer is applied and another electroplating process is used to produce the thermal contact pad and electrical bondpads as depicted in Fig. 5.

The lower thermal insulation (Module C) is fabricated with a backside DRIE process. The process parameters are optimised to yield negative side walls. This is necessary to create a large membrane while maintaining a large contact area for the bonding of a second wafer. The second wafer is bonded using a low temperature plasma bonding process [9].

Finally, the wafer is diced to 10x10mm² chips using a wafer saw.

3.3 Device Testing

After a gross functional test, only single rows of 125 thermocouples were found operable and are further characterized instead of a complete chip with 7500 thermocouples. Fig. 6 shows the setup for performance measurements. The chip is mounted on an Al chuck using a thermal conductive sheet (contact resistivity $K_{HC} = 0.5\ KW^{-1}$). A hot plate heats the chuck. The

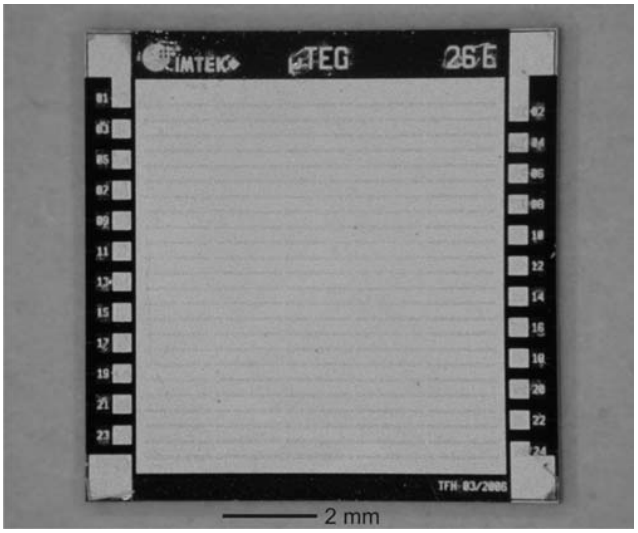

Fig. 5: Microscopic image of the meandering thermocouple structure.

top thermal contact is established using a pressure contact between the thermal contact pad on the front side of the chip and an Al cover plate. Literature data is used for a rough estimation of the top thermal contact resistivity K_{cc} of approximately $8.8\ KW^{-1}$. A Peltier cooler and a CPU fan cool the cover plate. The temperature difference is recorded with two PT 100 resistors embedded in the chuck and cover plate. Using the thermal contact resistances given above and the simulated thermal resistance of $1.55\ KW^{-1}$ for the generator device, the temperature difference across the chip ΔT_G is 14.3% of the measured value ΔT_{meas}. The measurement results of the output voltage are show in Fig. 7. Thus a linear temperature coefficient of $9.51\ mVK^{-1}$ is found.

4. DISCUSSION

The measurements above indicate an internal electrical resistance of 84 kΩ and an open-circuit voltage of $9.51\ mVK^{-1}$ for 125 thermocouples. Extrapolating these data to a device with 7500 thermocouples would lead to a resistance of 5.04 MΩ. This value is significantly higher than the simulated value of 0.383 MΩ. The major source for this deviation is the increased electrical resistance of the device due to problems in Al processing. Therefore, a device with 7500 thermocouples would have a device power factor of $1.612 \cdot 10^{-4}\ \mu Wmm^{-2}K^{-2}$, compared to the simulated value of $3.63 \cdot 10^{-3}\ \mu Wmm^{-2}K^{-2}$.

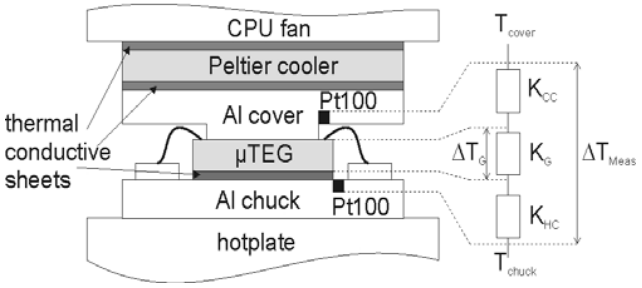

Fig. 6: Schematic of the measurement setup. The thermal network on the right-hand side indicates the contact resistances that consume 85.7% of the measured temperature difference.

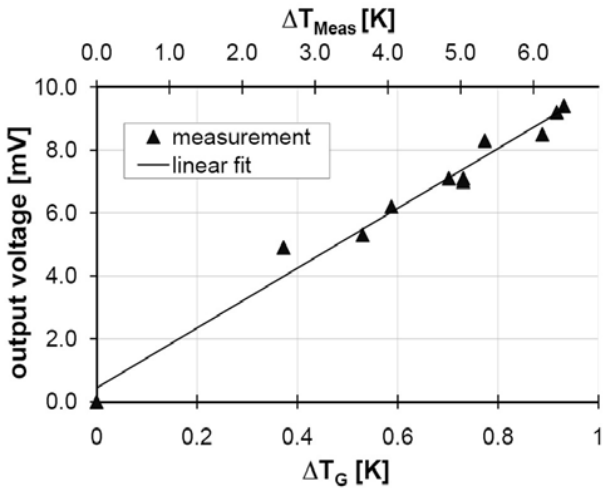

Fig. 7: Measured open-circuit voltage of 125 thermocouples.

5. CONCLUSION

An output power in the µW range is of increasing interest for the supply of ultra-low power CMOS electronics, which would allow the combination of µTEGs with distributed and embedded microsystems. Within this paper, a novel way of manufacturing thin-film based micro thermoelectric generators is evaluated. A functional prototype is fabricated and measurement results prove the feasibility of the concept. Further work is required to optimize the performance of the generator using superior thermoelectric materials such as BiSbTe compounds.

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