INNOVATING TECHNOLOGICAL APPROACH FOR SI-SIGE SUPERLATTICES INTEGRATION INTO THERMOELECTRIC MODULES

G. Savelli¹, M. Plissonnier¹, V. Remondière¹, J. Bablet¹, J.M. Fournier¹,²
¹ Laboratoire des Composants Hybrides, CEA-Liten, Grenoble, France
² Laboratoire de Génie Electrique de Grenoble, UMR 5269-CNRS, St-Martin-d’Hères, France

Abstract: This paper presents the development of doped polycrystalline Si-SiGe superlattices as thermoelectric (TE) elements integrated into generators. Modules dimensions are 1 cm², Si and SiGe are in-situ doped (n and p types) and realized by CVD (Chemical Vapor Deposition) on 4 inches (001) silicon wafer. Si-SiGe superlattices growth will be studied, as well as their integration into thermoelectric modules. Interest of using superlattices as TE materials will be justified by their thermal conductivity measurements. Moreover, process fabrication and different geometries design will be presented. Finally, first measurements realized on these modules allowed scavenging 320 mV for a temperature difference of 90K.

Key Words: thermoelectric generators, Si-SiGe superlattices, thermal conductivity, Seebeck voltage.

1. INTRODUCTION

Since the last decade, there is a growing interest in wireless sensor nodes with the goal of monitoring human environments. Because advances in low power VLSI design and CMOS fabrication have dramatically decreased power requirements of sensors, it is now possible to consider self-powered systems in sensor nodes [1]. At the same time, the interest in producing micro-electromechanical systems (MEMS) opens new opportunities in the field of micro power generation. Micro thermoelectric converters are a promising technology due to their high reliability and quiet operation, and the fact that they are usually environmentally friendly.

Nanostructured thermoelectric materials are in their way to revolutionize the fields of thermoelectric cooling and energy conversion. In particular, thermoelectric power generation is a clean energy source, and it is ideal for waste heat recovery applications.

Thermoelectric materials are classified by their dimensionless figure of merit ZT defined by:

\[ ZT = \frac{\sigma S^2}{\lambda T} \]  

As shown in equation 1, to obtain high ZT values, it is necessary to have high power factor \( \sigma S^2 \) and low thermal conductivity \( \lambda \). Moreover \( \lambda \) is the sum of two distinct contributions: the lattice contribution \( \lambda_l \) and the electronic contribution \( \lambda_e \) defined as follow:

\[ \lambda_e = L_0 \times \sigma \times T \]  

where \( L_0 \) represents the Lorentz number. Equation 2 shows that it is not possible to decrease \( \lambda_e \) without decreasing \( \sigma \) too. So the only possibility is to decrease the lattice contribution \( \lambda_l \), characterized by the phonon transport. That is why, in recent years, a lot of work on superlattices had been studied [2]. Advantages on thermal conductivity decrease and power factor increase are well-known. Indeed phonon diffusion on Si-SiGe interfaces leads to a decrease of lattice thermal conductivity and a potential increase of figure of merit ZT. But today, despite all these works, it is uncommon to find global TE devices integrating these structures in literature. Thus, after the development of thermoelectric generators based on bismuth and antimony elements [3], we present here thermoelectric modules based on Si and SiGe superlattices.

2. EXPERIMENTAL

2.1 Si-SiGe superlattices growth

Si and SiGe layers are grown by reduced pressure chemical vapor deposition (RP-CVD). This deposition technique has been already used...
in literature to realize superlattices [2, 4-5]. CVD offers high layers quality and makes possible to use in-situ doping. The growth pressure was always 10 Torr. The flow of H₂ carrier gas was set at a fixed value of about one ten of standard liters per minute. Pure silane (SiH₄) was used as the source of Si and germane (GeH₄) diluted at 10% in H₂ as the source of Ge. Doping sources are diborane (B₂H₆) and phosphine (PH₃) diluted at 1% in H₂ as p- and n-type respectively.

All experiments were realized using (001) Si wafers. Moreover, SOI (silicon on insulator) substrates were used for devices development (section 3) to minimize heat conduction through the substrate.

Before each layer growth, the initial step consisted in removing the surface native oxide by an in-situ thermal treatment at high temperature under H₂ flow during 10 minutes.

Germanium stoichiometry in SiGe layers was controlled by X-ray diffraction (XRD) and fixed at 15%. Doping levels were controlled by SIMS (secondary ion mass spectrometry) measurements and fixed at 10²⁰ at.cm⁻³.

Moreover, layers interfaces and superlattices quality were controlled by SEM (scanning electron microscope) or TEM (transmission electron microscope) analyses.

Finally, thermal conductivity measurements were realized by 3ω method. This method has already been used for thermal conductivity measurements of Si-SiGe superlattices [6].

2.2 Interest of superlattices

We have realized several Si-SiGe superlattices with different periods and crystallographic structures. The objective is to note the influence of these superlattices on thermal conductivity.

Characteristics of tested superlattices are summarized in table 1.

Polycrystalline and monocrystalline samples were grown at 700°C and 1000°C respectively. Total superlattices thickness is 300 nm, in agreement with 3ω method specifications.

To illustrate the samples, SEM images are given in figure 1. Figure 1-a represents a monocrystalline structure with a 20 nm (Si) and 20 nm (SiGe) period (sample SL2). Figure 1-b represents a polycrystalline structure with an 8 nm (Si) and 8 nm (SiGe) period (sample SL5).

<table>
<thead>
<tr>
<th>Sample number</th>
<th>Crystallographic structure</th>
<th>Period Si-SiGe (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SL1</td>
<td>monocrystalline</td>
<td>40-40</td>
</tr>
<tr>
<td>SL2</td>
<td>monocrystalline</td>
<td>20-20</td>
</tr>
<tr>
<td>SL3</td>
<td>monocrystalline</td>
<td>8-8</td>
</tr>
<tr>
<td>SL4</td>
<td>monocrystalline</td>
<td>4-8</td>
</tr>
<tr>
<td>SL5</td>
<td>polycrystalline</td>
<td>8-8</td>
</tr>
</tbody>
</table>

Table 1: Crystallographic structures and Si-SiGe period of tested superlattices.

Fig 1: SEM images of: a- monocrystalline Si-SiGe superlattice (sample SL2); b- polycrystalline Si-SiGe superlattice (sample SL5).

The five structures defined in table 1 have been characterized by 3ω method to observe the influence of superlattices period on thermal conductivity λ. Results are given in table 2.
Table 2: Thermal conductivity of Si-SiGe superlattices defined in table 1, measured by 3ω method.

<table>
<thead>
<tr>
<th>Sample number</th>
<th>$\lambda$ (W.m$^{-1}$.K$^{-1}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SL1</td>
<td>14</td>
</tr>
<tr>
<td>SL2</td>
<td>7</td>
</tr>
<tr>
<td>SL3</td>
<td>5.4</td>
</tr>
<tr>
<td>SL4</td>
<td>5</td>
</tr>
<tr>
<td>SL5</td>
<td>2.8</td>
</tr>
</tbody>
</table>

From table 2, we can see clearly the influence of superlattices period on thermal conductivity, with a decrease of $\lambda$ by decreasing period. Thus, figure 2 shows the evolution of $\lambda$ as a function of interfaces number per micron, obtained from results given in table 2.

![Graph showing the evolution of thermal conductivity $\lambda$ as a function of interfaces number in superlattices.](image_url)

Fig 2: Evolution of thermal conductivity $\lambda$ as a function of interfaces number in superlattices.

The curve appearance shows once more a decrease of $\lambda$ with the period, and is in agreement with literature [6].

Moreover, if we consider, for example, sample SL3, we would have to obtain a $\lambda$ of 12 W.m$^{-1}$.K$^{-1}$ according the Fourier law; however we obtain 5.4 W.m$^{-1}$.K$^{-1}$, emphasizing the influence of these nanostructures.

At last, if we compare samples SL3 and SL5, they have the same period (8nm-8nm) but the first one is monocrystalline whereas the second one is polycrystalline. We can see that thermal conductivity decreases by a factor 2 using polycrystalline structures. The main reason of this difference is due to phonon scattering at grain interfaces [7-8].

3. SL INTEGRATION AND RESULTS

Si-SiGe superlattices are now going to be integrated into thermoelectric modules. For that, we use a four inches SOI wafer. 42 devices and 6 test areas are distributed on it. Figure 3 shows this prototype.

![Image of Si-SiGe superlattices integrated into thermoelectric modules, realized with microelectronic technologies.](image_url)

Fig 3: Si-SiGe superlattices integrated into thermoelectric modules, realized with microelectronic technologies.

Dimension of chips is 1x1cm$^2$, superlattices line widths are 40 or 60 μm, spaced by 20 μm. Final device is obtained after several steps of deposition, etching and annealing. This geometry allow us to obtain 166 lines (83 of n-type and 83 of p-type in alternation), i.e. 83 junctions for the 40x20 chips, 124 lines and 62 junctions for the 60x20 chips. Moreover n-type and p-type superlattices lines are electrically connected in series by using Ti and Pt metallic junctions. Figure 4 shows these lines and metallic connections more in details. Superlattices used in this device are the polycrystalline superlattices, having the lowest thermal conductivity (SL5: 8 nm Si and 8 nm SiGe). Superlattices thickness is 3 μm whereas metallic connections thickness is 500 nm. Figure 5 shows the n- and p-type lines in cross-section, with an enlargement of superlattice.

We measured Seebeck voltage by applying a temperature difference at the two extremities of module. For that, we have heat one extremity of lines and cooled the other one using a specific and adapted characterization tool.
Fig 4: SEM image showing n- and p-type Si-SiGe superlattices lines electrically connected (sight top picture).

Fig 5: SEM images showing lines of Si-SiGe superlattices (a) with an enlargement of superlattice (b).

4. CONCLUSION

We developed thermoelectric modules using Si-SiGe superlattices. We tested several superlattices with different crystallographic structures (poly- or monocrystalline) and different period. We measured thermal conductivity of 2.8 W.m⁻¹.K⁻¹ for polycrystalline 8 nm (Si) – 8 nm (SiGe) superlattices. Then, we integrated this superlattice into specific thermoelectric module and measured a promising Seebeck voltage of 320 mV for a temperature difference of 90K. Some improvements are currently tested to increase performances.

REFERENCES